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1 Introduction

The European R&D project *Direct Current Components + Grid* (DCC+G) aims to develop innovative power semiconductors and products using them to increase the energy efficiency of commercial buildings. Hereby the partners of the project aim to contribute to the realization of the European Commission target that all new buildings in the EU shall be constructed as zero-energy buildings latest 2021 [1]. Examples of such buildings illustrate that electricity will replace fossil fuels in many energy related processes of such buildings [2]. Thus the cost effective and energy efficient use of electricity in buildings is an import area for technical innovations in the 21st century.

A 2-phase (or 1-phase) low voltage direct current (DC) grid with supply voltages of ±380 V (or 380 V) offers benefits compared with a 3-phase 400 V AC (or 1-phase 230 V AC) grid supply, which are used internally in many modern electrical appliances. Electricity from a DC supply can be controlled more flexible, with higher performance and efficiency, at lower cost than from AC electricity sources.

Due to the fact that DC grids lack a voltage zero-crossing point in the voltage characteristic, electric arcs following switching operations or failures are not cleared consequently like in AC grids. Therefore, it is necessary to develop an arc management system using power electronics to ensure a safe operation of the DC grid under any circumstances. Part of it could be a method that immediately switches of the central DC bus to clear the arc after its detection for a certain period of time. After this short break the system voltage is switched on again and it is verified if the arc is cleared. If the arc is still burning the DC voltage must be switched off again and should remain in the off-state. This report focuses on common methods to detect arcs in DC grids and some basic simulations are run to define the time for the short breaks and to gain knowledge about the input capacitance of the devices to inhibit oscillations and to override the short break time.

Moreover, the proposed DC supply grid bears special requirements for the used power electronics topologies. Several conventional topologies to connect energy storages or photovoltaic generators to the main grid are not applicable with the proposed DC grid architecture. An objective discussion is consequently needed to solve the problems connected with this issue.

2 BASICS OF ELECTRIC ARC PHYSICS

An electric arc is an electrical breakdown of a gas which produces an on-going plasma discharge, resulting from a current through normally nonconductive media such as air. An arc discharge is characterized by a lower voltage than a glow discharge, and relies on thermionic emission of electrons from the electrodes supporting the arc [3].

Figure 1 shows an example DC circuit to illustrate the switching behavior in an ohmic-inductive load circuit.

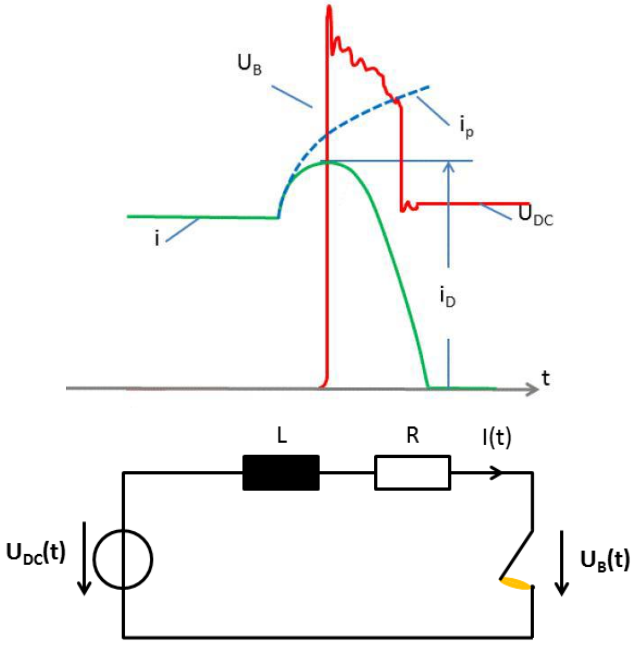

Figure 1: Ohmic-Inductive circuit with switching arc and principle voltage and current dependencies (picture source: [4])

The mathematical equations to compute the curve shapes of the variables are as follows:

$$U_{DC} = R * i\ t\ + L * \frac{\partial i\ t}{\partial t} + U_B(t), \quad (1)$$

$$i\ t\ = \frac{U_{DC}}{R} - \frac{U_B\ t}{R} * \ 1 - \exp(-\frac{t}{\tau}) \quad (2)$$

with U_B: arc voltage; U_{DC}: source voltage; i_P: prospective current (U_{DC}/R); i_D: let-through current.

Considering methods to clear the electric arc in a DC grid after a switching action, one has to take a closer look at the physical principle of the arc. **Figure 2** illustrates the curve shape of the electric potential across an electric arc between two electrodes.

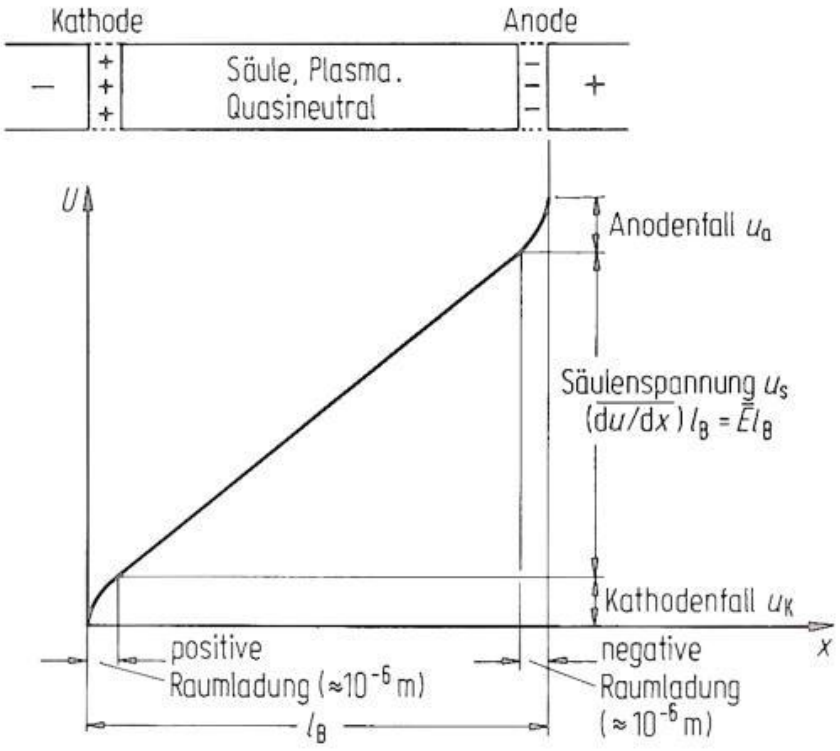

Figure 2: Simple Model of the electric potential across an electric arc (picture source: [5])

The arc voltage U_B for steady state can simply be computed with the Ayrton equation:

$$U_B\ l, I_B\ = a + b * l + (c + d * l)/I_B \tag{3}$$

with U_B, I_B, l: arc voltage; current and length; a: V_A+V_C, sum of cathode and anode fall (minimum voltage of the arc); b: electric field strength; c, d: parameters dependent of the used material.

An electric arc only burns stable if the value of the arc current lies over a limiting minimal current value. Therefore Eq. (3) is extended with this minimal value to Eq. (4):

$$U_B\ l, I_B\ = a + b * l + (c + d * l)/(I_B - I_{B,min}) \tag{4}$$

The resulting curve has the shape of a hyperbola and can be seen in **Figure 3**.

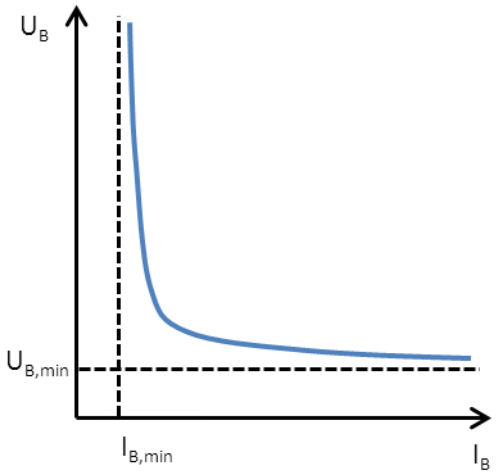

Figure 3: Resulting curve of an electric arc (picture source: [5])

Transferring this knowledge to the ohmic-inductive circuit of **Figure 1,** one can see that the arc is extinguished when the arc voltage exceeds the source voltage. This procedure is demonstrated in **Figure 4.** In this example the curve shapes of the system variables are shown for the opening of the contacts of a mechanical relay with the development of the arc and its extinguishment.

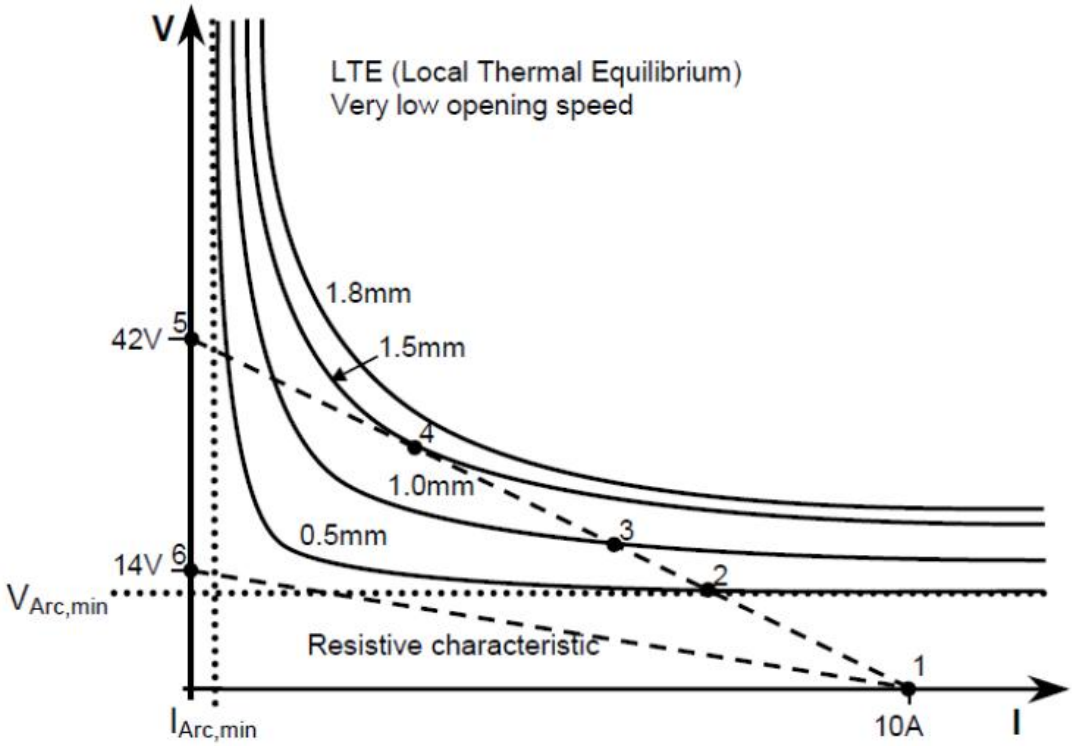

Figure 4: Opening of a mechanical relay with the different operating points (picture source: [18])

In point 1 the contacts are closed, so there is no arc. By opening the contacts the operating point jumps onto the characteristic curve of the arc which varies with the increasing distance between the opening contacts. The wider the contacts open the

higher the resistance of the arc column becomes, so the current drops and the voltage over the arc increases to the values of the points 3 an 4. As soon as the arc voltage exceeds the source voltage the arc extinguishes and point 5 is reached.

3 SWITCHING DC CURRENTS

The possibilities to switch DC currents are manifold and depend on the requirements given in each case. Principally, there are three different physical principles to realize a switch. Those are mechanically, electrically and a hybrid version.

3.1 SWITCHING DEVICES WITH MECHANICAL CONTACTS

The common technique used in mechanical switches is to increase the arc voltage by splitting the arc into several smaller arcs. This is done by so called splitter plates. The arc is forced into the arc splitting chamber via the magnetic Lorentz force which is generated by a permanent magnet. The setting of such a mechanical circuit breaker is shown in **Figure 5**.

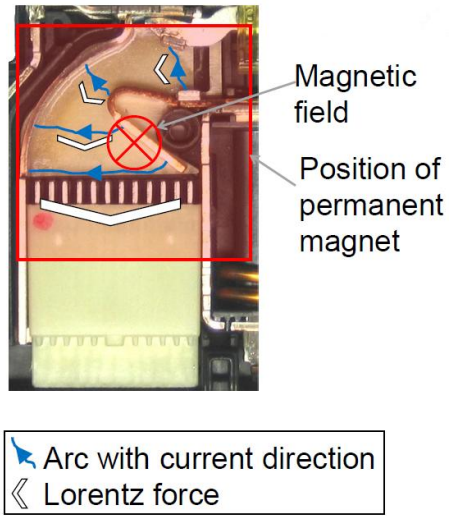

Figure 5: Setting of a mechanical circuit breaker (picture source: [4])

The effect of increasing the arc voltage by splitting is displayed in **Figure 6**.

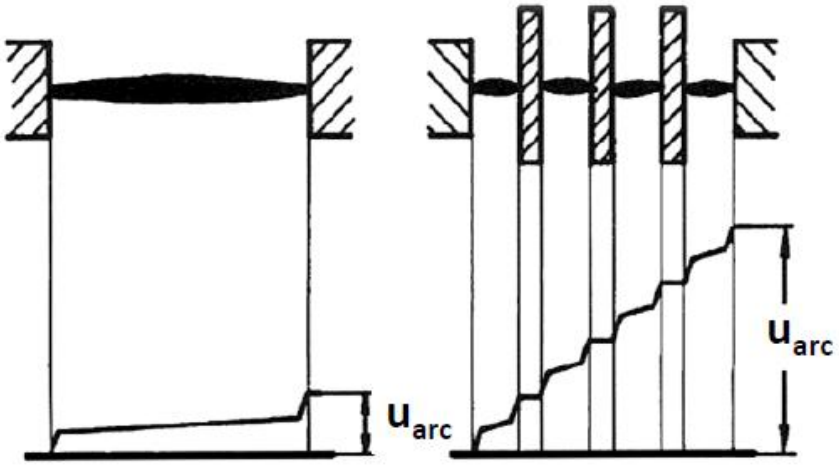

Figure 6: Increasing the arc voltage by splitting (picture source: [4])

To support the extinguishing procedure and to enable a small scale of the circuit breaker switching chambers, filled with gas are applied. **Table 1** gives an overview of some properties of established gases used in molded case circuit breakers. In addition to the gases, the values of vacuum are presented.

Table 1: Properties of common used gases and vacuum in molded case circuit breakers [4]

	Thermal Conductivity [W/m*]	Molar Mass [g/mol]	Oxidation Protection of the contacts necessary?
Vacuum	0	0	yes
Air	0.0262	28.97	no
H_2	0.1861	2.016	yes
N_2	0.026	28.2	yes
SF_6	0.0135	146.05	yes

Every single gas mentioned in the table has its advantage in using it as a switching media. For example, H_2 is able to cool the arc very fast and is thus enabling short extinguishing times, N_2 is able to provide a high dielectric strength, Vacuum has no particles to be ionized till metal is vaporized an SF_6 provides high ionization energy. It is strongly depending on the application which gas is used as the switching media in the circuit breaker. **Figure 7** shows the setting of a molded case circuit breaker filled with hydrogen gas.

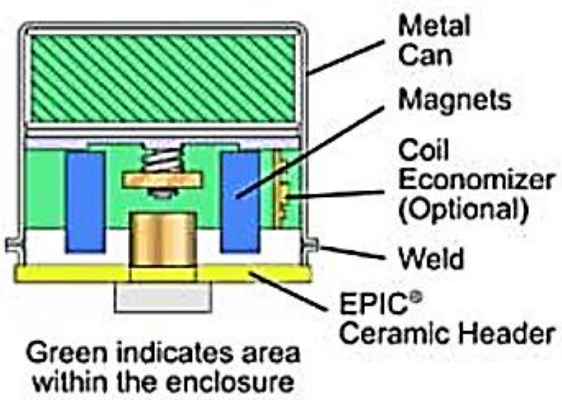

Figure 7: Setting of molded case circuit breaker filled with hydrogen gas (picture source: [4])

The switching time of a mechanical circuit breaker strongly depends on the gas used as the switching media. Measurements done by E-T-A have shown that the fastest switching time is achieved when a mixture hydrogen and nitrogen is used as the filling gas of the switching chamber with a certain mechanical design of the switching device [4]. The switching time strongly depends on the dynamic behavior of the mechanics. The gas mixture is only one influencing parameter.

3.2 SWITCHING DEVICES WITH POWER ELECTRONICS

Using power electronic switches like MOSFETs or IGBTs has the advantage of a limited current peak because of the reduced ampacity of electronic power switches. The maximum current is limited to a defined value (typically 1.5 to 2 times rated current). The current does not rise to the same high values like in mechanical

switches. This also results in a smaller i^2t-value and almost no voltage breakdown of the supplying bus voltage. The switching curve of a mechanical and electronic circuit breaker within a 24 V automotive on-board supply system can be found in **Figure 8**.

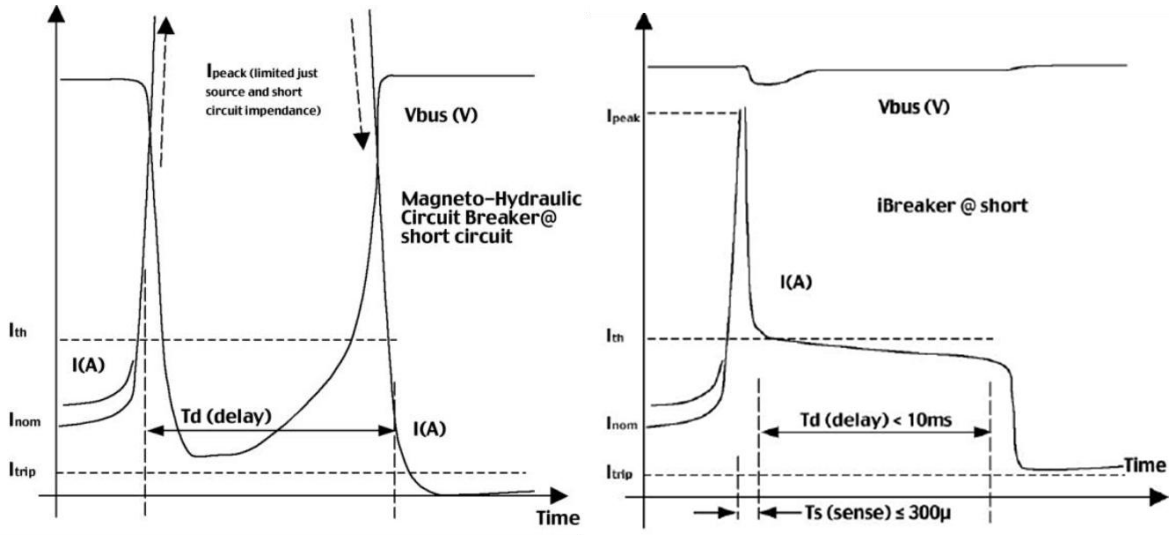

Figure 8: Measured curves for switching operation with mechanical (left) and electronic power switch (picture source: [4])

Whether power electronic switches are also feasible for switching operations with higher voltages like the proposed ± 380 V_{DC} system at DCC+G, needs to be specially determined and revised. Typically, power electronic switches are not used to clear short circuit faults. Often it is indispensable for power switches to provide a certain degree of galvanic isolation against electrical breakdown, which also cannot be provided by power electronic switches. Further research in this field is consequently needed. As well the power losses in ON-state are a criterion, which has to be considered when developing an electronic switch.

3.3 HYBRID SWITCHES

A possible way to combine the advantages of a mechanical switch with the ones of a power electronic switch is presented in this subsection. As an example, an AFCI with arc detection unit (see section 5), a product of E-T-A GmbH, is described. The device is a hybrid switch, combining a mechanical with a semiconductor switch. **Figure 9** shows the simplified schematic. By actuating the disconnection, switches S1, S2 and S3 will be opened followed by the occurrence of an arc between the contacts of S1. If the resulting potential difference reaches a value of approximately 16 V the power semiconductor device will connect through and entirely take over the current. This will cause extinguishing the arc over S1. The power semiconductor switch now turns off the current in a defined way and the mechanical contacts continue to open without current. Of course, this will significantly prolong durability and endurance of the device.

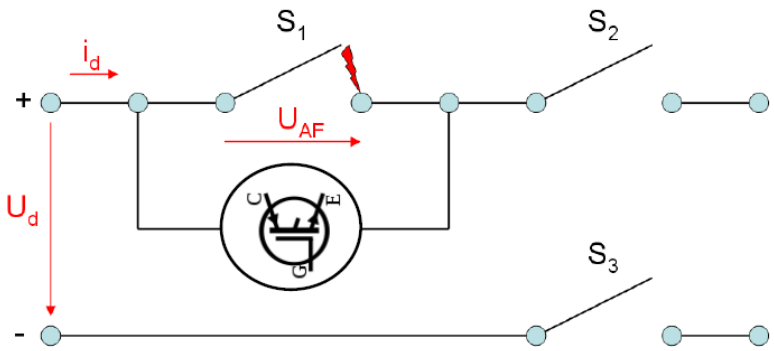

Figure 9: Schematic of hybrid switch (picture source: [4])

The curves of a switching operation with and without a power semiconductor switch are displayed in **Figure 10**. The values of voltage and current are selected to 750 V_{DC} and 4.5 A respectively. From the curve progression one can see that through the use of a semiconductor switch the speed of the switching operation is increased and dissipated energy is therefore minimized.

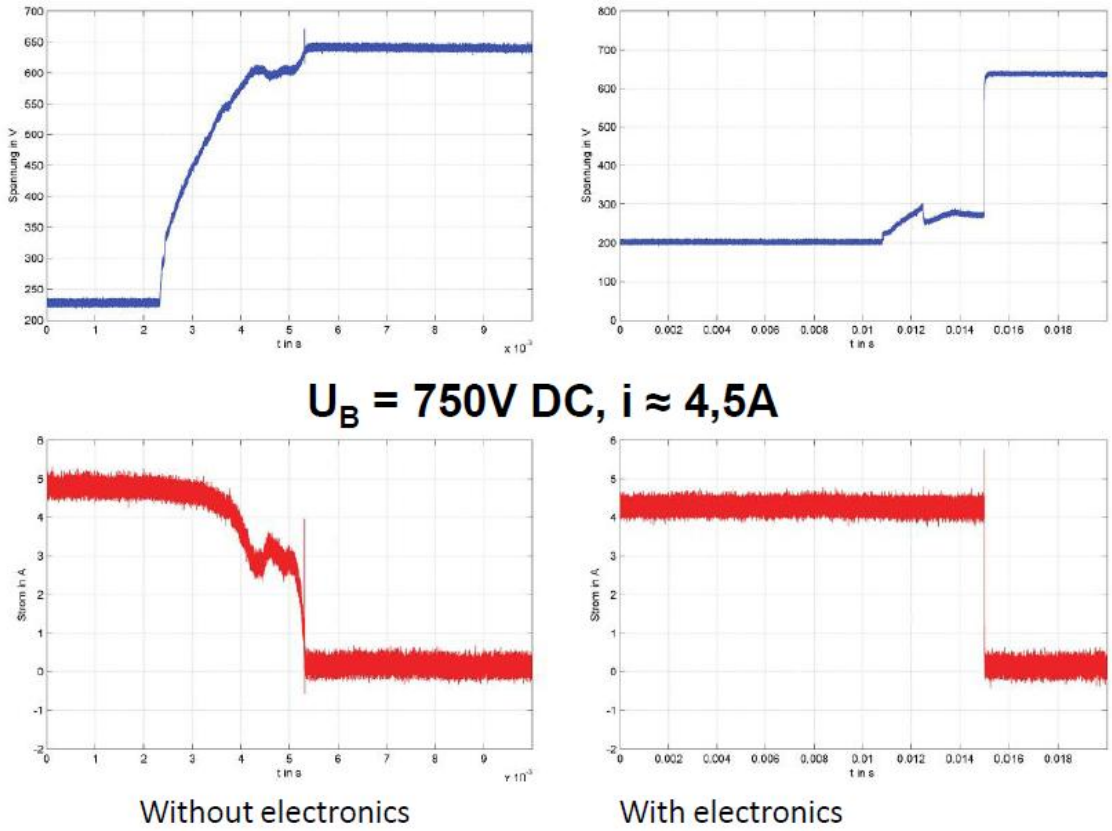

Figure 10: Curve progression of switching operation performed at 750 VDC and 4.5 A with and without semiconductor power switch (picture source: [4])

In **Figure 11** the described hybrid switch is shown. The device is constructed for top hat rail mounting and can therefore be installed close to pv-system itself. The device presents an all-in-one solution which includes the arc detection unit, the hybrid circuit breaker and a remote emergency switch.

Figure 11: Hybrid circuit breaker for top hat rail mounting (picture source: [4])

The resulting setup for the proposed grid architecture with the circuit breakers, arc detection unit and the described emergency switch is displayed in **Figure 12**.

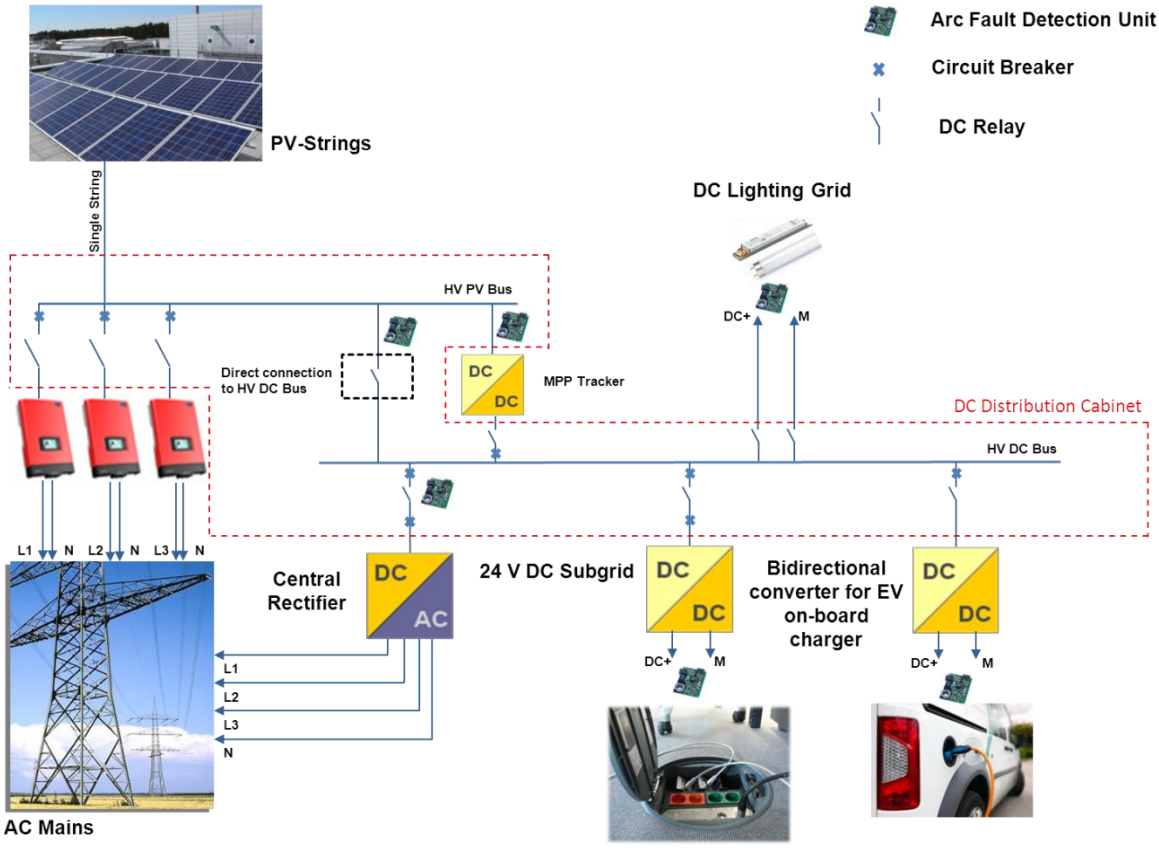

Figure 12: Proposed DC grid architecture with arc detection unit and circuit breakers

Of course, appropriately dimensioned circuit breakers are needed additionally in each branch of the microgrid to guarantee a safe switch-off in case of a fault.

4 HAZARDS OF ARC FAULTS IN DC SYSTEMS

Fault arcs are exorbitantly critical in any kind of DC system, because their occurrence can result in fire or electric shock which can have lethal consequences for the human and animal body.

The hazard potential of fault arcs is well studied especially in photovoltaic systems. Reasons for the occurrence in these kinds of faults are improper installation and planning of the system, deficient product quality and external intakes, like harsh weather conditions [6]. Fault arcs can now occur in consequence of mechanical stress due to snow load or stone-chipping, defective connecting boxes, damaged cables, bad quality connectors or flooding. Another critical factor is the aging of the panels which amplifies the before mentioned effects.

The following **Figure 13** portrays a fault arc in a junction box.

Figure 13: Burning fault arc in a connection box (picture source: [7])

As already mentioned, the system behaviour in case of a fault arc should not be very different between a pure pv-system and a low voltage DC microgrid. Like in pv-systems, all power electronic component, like the central rectifier or DC/DC converters, will contain overcurrent and overvoltage protection units and will probably be able to detect all kinds of fault arcs. For sensitisation, the next sections will give a brief introduction of possible arc faults in DC supply systems followed by a detailed description of the arc fault problem in pv-systems.

4.1 ARC FAULTS IN LOW-VOLTAGE DC MICROGRIDS

Thinking of possible locations for the occurrence of arc faults in DC supply systems, one has to differ between faults occurring on the central DC bus and faults occurring directly at the connected components. **Figure 14** shows various arc fault types.

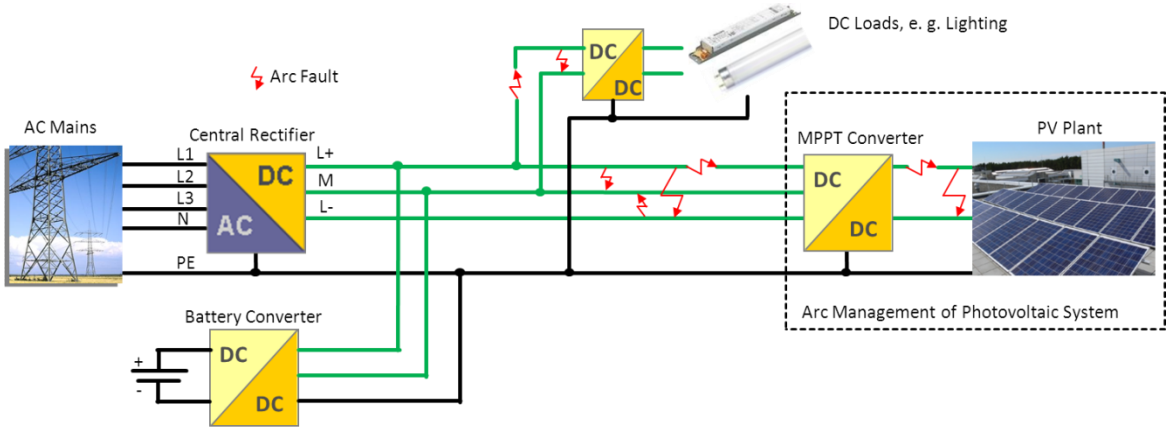

Figure 14: Various types of arc faults in low voltage DC microgrids

As can be seen from the figure, fault arcs either occur in series to a component of the microgrid or parallel to it. With regard to the detection of both fault types, the specific properties and their impact on the system variables can be used. This procedure is explained in detail for pv-systems in the following sections.

4.2 ARC FAULTS IN PHOTOVOLTAIC SYSTEMS

Conceivable locations for the occurrence of arc faults in PV-systems are [8]:

- parallel to solar inverter
- in series to solar inverter
- in series to panels in one string (typically up to approx. 20 panels in series)
- bridging one or more panels
- connection plugs between parallel strings
- from one string to another
- from any point to ground
- inside panel or inside its connection box

The following considerations mainly focus on the arc faults occurring in series and parallel to the solar inverter as displayed in **Figure 15** for they are the most likely occurring fault arcs in PV-systems.

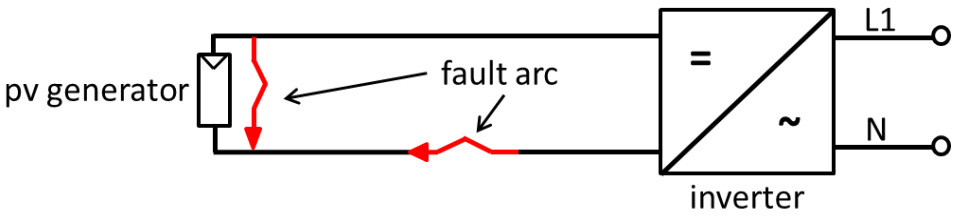

Figure 15: Series and parallel fault arc in a pv-system

In contrary to arc faults in automotive and aerospace applications (what means within a DC grid) the arc faults occurring in a PV-system are characterized by a varying

voltage depending on the irradiation on the panels and the constant load of the solar inverter over a wide operation range. Thus, in this context, the characteristic curve of the panel and the applied maximum power point tracking (MPPT) algorithm plays an important rule as will be described.

The depicted arc faults in **Figure 15** can be characterized as follows: A series fault arc is expected to be characterized by a lowered current caused by the additional resistance of the arc. Therefore, a conventional circuit breaker should not be able to detect and clear the fault, because it is generally designed to trip when operating parameters of the current are significantly exceeded. In contrary, a parallel fault arc is expected to be described by a very high current caused by the low ohmic connection between the high potential difference between the conducting phase and the neutral conductor. In consequence, the detection and clearance of a parallel fault arc might be easily achieved by a conventional circuit breaker. Both assumptions need to be proven in section **4.2**.

The main focus of attention is consequentially the detection of the series fault arc. The hazard for the system is strongly dependent on the maximum power point tracking control algorithm applied in the dc/dc-converter of the system. If the input voltage is stabilized to a constant value or the input capacitance of the converter is comparably high, then the pv-panels are forced to increase their voltage value. Thus, the point of maximum power will be left quickly and the value of the current flowing through the panels is decreased. This means that the clearance of the arc is supported by the control algorithm of the converter. On the other hand, if the input current of the converter is controlled or the input capacitance of the converter is of low value, then the input voltage of the converter will decrease slowly. In this case, the abandoning of the maximum power point will also take longer. The power absorbed by the arc increases in return what leads to a higher hazard potential [4]. **Figure 16** illustrates the two cases.

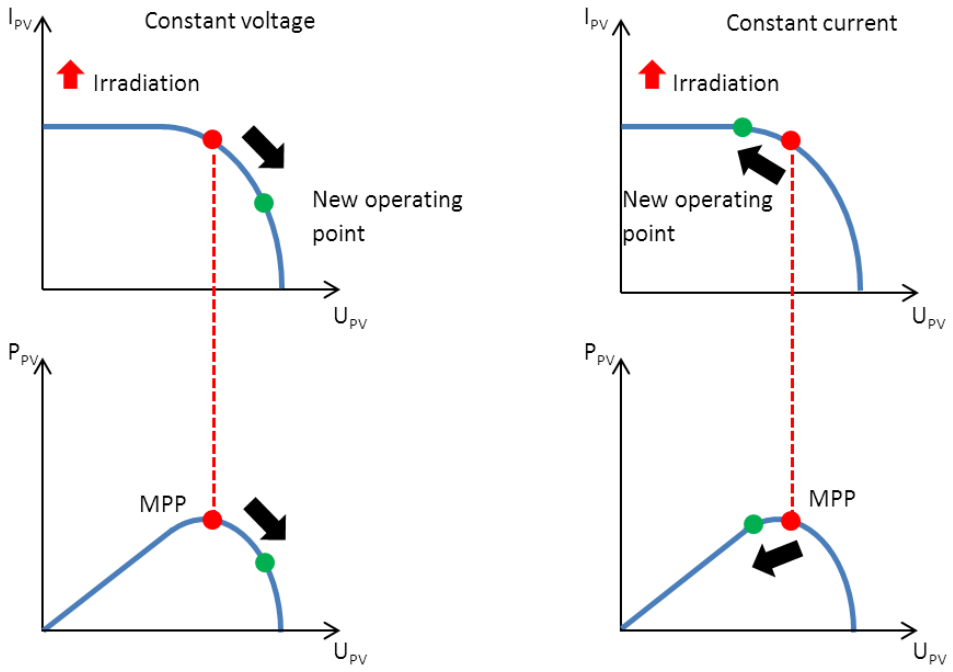

Figure 16: Influence of the converter control algorithm in case of a series fault arc (picture source: [6])

4.3 EXPERIMENTAL RESULTS FROM A TEST SETUP

In [8] a test setup for the measurement of arc faults in PV-systems is presented consisting of six panels connected in a row, an inverter, shunt resistors for current measurement, probes for voltage measurement and a variable gap device to create arc faults at different locations. The make-up of the test set-up can be seen in **Figure 17.**

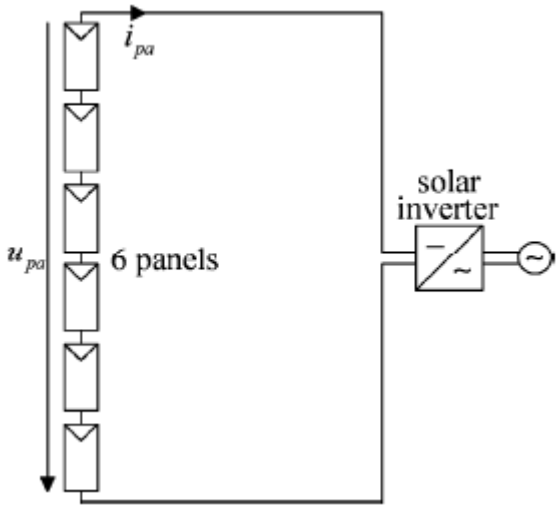

Figure 17: PV-system test setup schematic (picture source: [8])

The characteristic curve of the series connection of the six panels is given in **Figure 18**. Of course the voltage over the panels depends on the solar irradiance and the temperature of the panels.

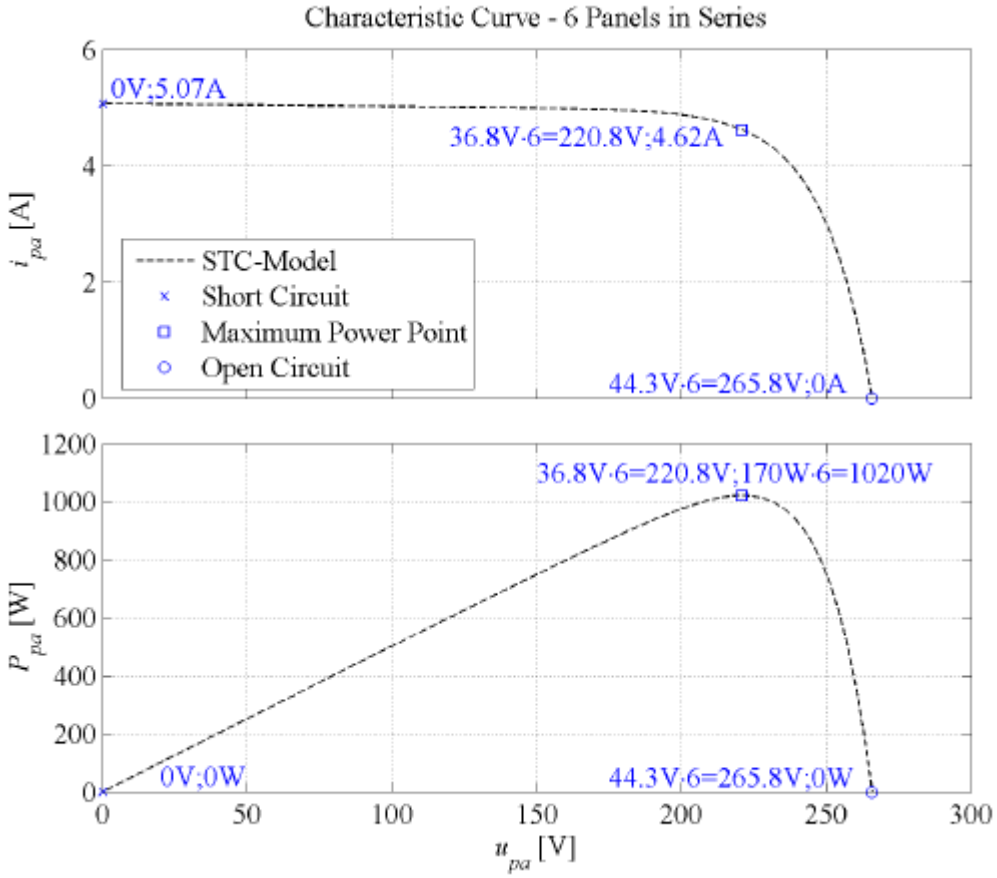

Figure 18: Characteristic curve of the six panels in series connection (picture source: [8])

In the following two sections the curves for parallel and series arc faults are presented.

4.3.1 PARALLEL ARC FAULT

The parallel fault arc is simulated by short-circuiting the string of PV-panels via a current-limiting ohmic resistor and the described arc fault device (**Figure 19**). The resulting arc is energized from two different sides. In the beginning, the energy to hold up the arc is supplied by the discharging input capacitor of the solar inverter for a certain time. This results in a change of sign for the input current of the inverter i_{iv}. After that, the fault arc is fed entirely from the pv-panels. The burning period of the arc now depends on the irradiation and the voltage level of the string of PV-panels. In cases of high irradiation and voltages, the arc burning can continue for a long time if the isolating distance of the fault arc device is not increased any further. This of course, increases the risk of damage [8]. **Figure 20** and **Figure 21** show the measured curves in case of low and high irradiation.

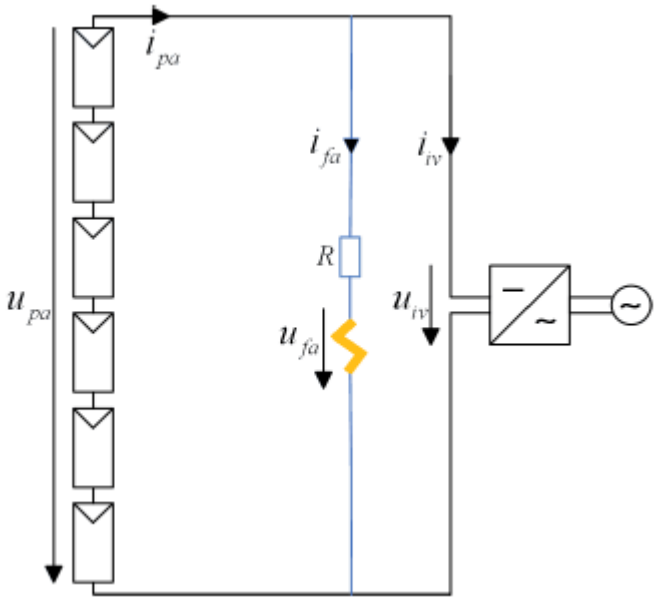

Figure 19: Parallel arc fault in test setup (picture source: [8])

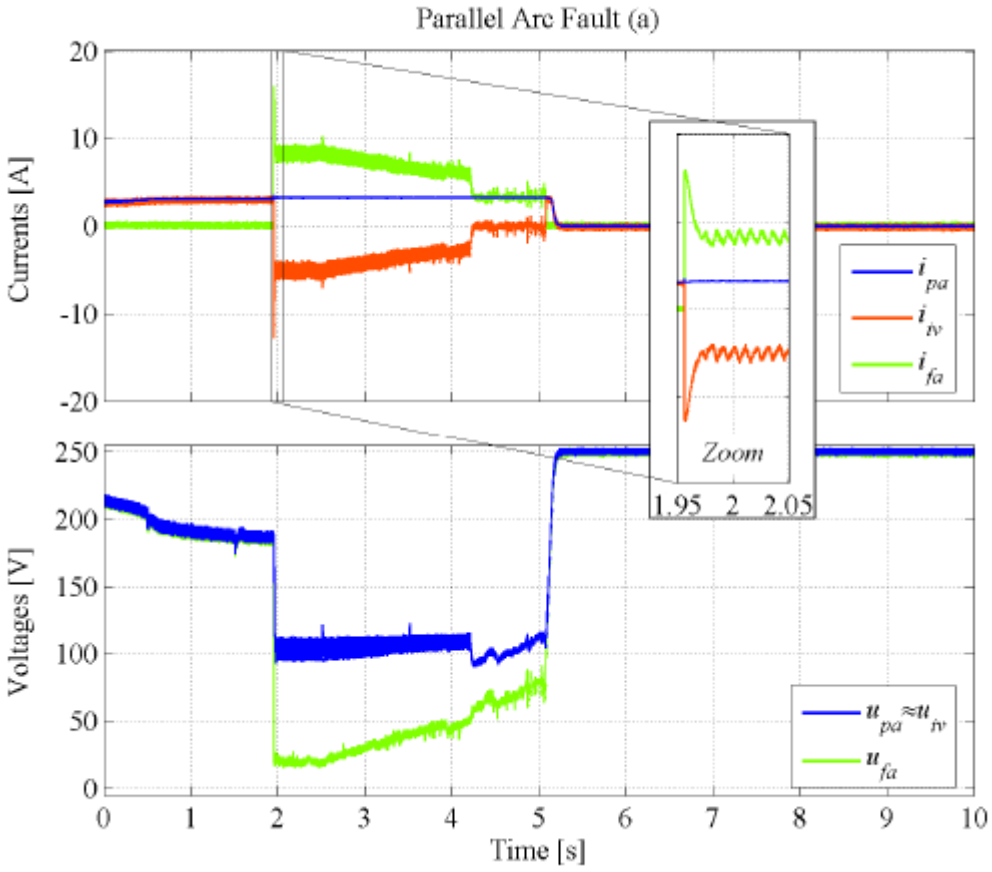

Figure 20: Voltage and current curves for parallel fault arc and low irradiation (picture source: [8])

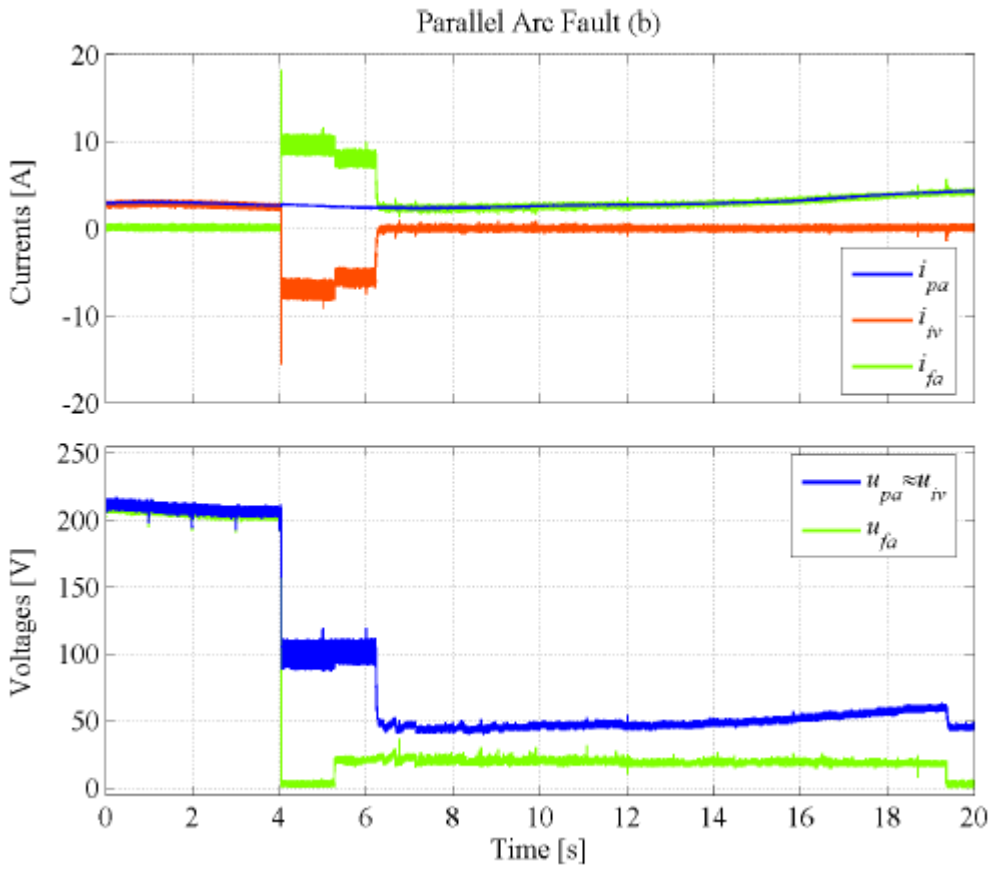

Figure 21: Voltage and current curves for parallel fault arc and high irradiance (picture source: [8])

Thinking of possible arc detection devices one can say that for the detection of the parallel fault arc no such devices or additional sensors are necessary, because the parallel fault arc can be detected when the input current of the solar inverter changes its sign. Therefore, an easy way to clear this type of fault arc is an inner inverter short circuit, which causes the arc to extinguish.

4.3.2 SERIES ARC FAULT

An entirely different situation emerges if the fault arc emerges in series to the pv-generator which presents the more likely type of fault for it occurs mostly in the connectors and plugs of an aged system.

The equivalent circuit diagram of the test case with arcing fault condition is shown in **Figure 22**. The system is considered to be working at its maximum power point at the time when the arc occurs.

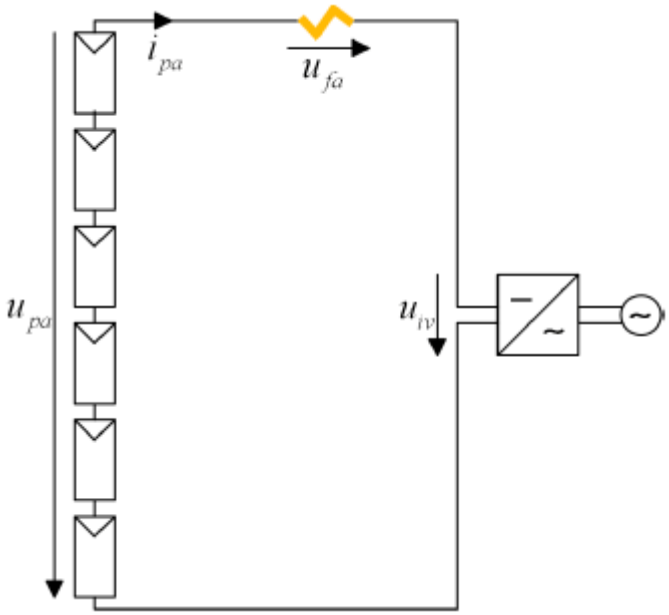

Figure 22: Setting of series fault arc in the test case (picture source: [8])

As it can be seen in **Figure 23** the current i_{pa} and the voltage u_{iv} will decrease slightly whereas the string voltage u_{pa} increases. This means that the panels are working at a lower power level after the arc occurs. But, all in all, the measured changes of the system variables after the start of arcing are really small compared to the changes measured in case of a parallel fault arc.

This means that measuring the input voltage and input current of the inverter is not sufficient to detect the arc due to its low sampling rate [8]. For this reason, other properties of the measured current and voltage signals need to be considered for the detection of a series fault arc.

In **Figure 23** the signal named sensor voltage is gathered with an inductive coupled sensor device capable to analyse a band of frequencies up to 2 MHz [8]. The signal can be used to detect the arc and to trip safety and clearing devices. But also other possibilities to detect series fault arcs exist as it will be explained in section 5.

For a more profound analysis on more fault situations in PV-systems see [8] and [9]. The following section 5 deals with several applied methods to detect fault arcs based on the different physical properties of the arc plasma.

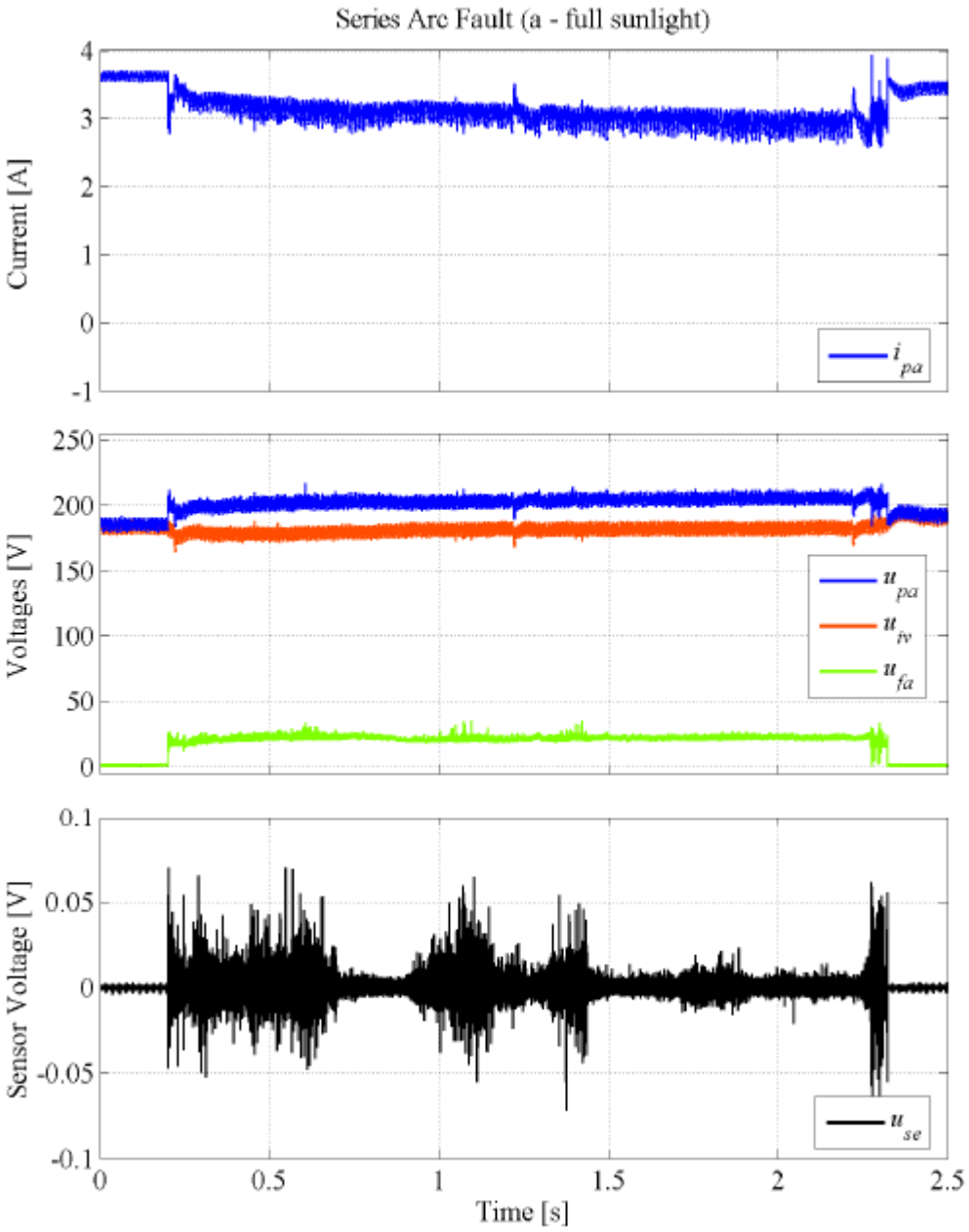

Figure 23: Series fault arc when operating at maximum power point (picture source: [8])

5 METHODS OF FAULT ARC DETECTION

If the arc emerges out of a fault condition it is very important to detect the arc and clear it as soon as possible. It is furthermore necessary that the other loads and sources of the connected grid will not be affected by the fault condition and can return to normal operation quickly. If the arc emerges out of a fault the exact type of the fault, e. g. short circuit between line and earth or short circuit between two lines, has a significant influence on the voltage and current curve of the system. A detection system for arcs must be able to decide which type of arc is detected and which action of the grid controller or safety devices must be performed to clear the arc.

For the detection of the arc different methods are available. Each method focuses on different physical properties of the arc, those are:

- the emitted acoustic noise of the burning arc
- the optical emission
- the rise of temperature (arc temperature around 10000 K)
- the noise component of the arc in the frequency spectrum of current and voltage

Each detection method has its own advantages and disadvantages as will be pointed out in the following subsections.

5.1 ACOUSTIC NOISE DETECTION METHOD

The method is based on the same physical principle like thunder. The heat of the emerging arc causes an instantaneous rise of the pressure of the surrounding air. The air molecules are accelerated and breakthrough of the sonic wall.

Methods focusing on the detection of the acoustic noise use piezoelectric sensors to measure the steep rise in pressure. The method is characterized by its high cost and high complexity. The needed piezoelectric sensors must be located near the potential fault locations. Accurate acoustic filters are needed additionally in noisy environments. The usability for this detection method is consequently low.

5.2 OPTOELECTRONIC DETECTION METHOD

Optoelectronic detection uses the emitted radiation of the arc. Either photodiodes or special cables with optical conductive coatings which must be able to withstand the same electrical loading like the insulation of a conventional cable are used for the detection units. **Figure 24** shows the make-up of such a cable.

The signal is then detected via an optoelectronic coupler. Every electrical junction in the system must therefore be equipped with the additional optical system. But unfortunately, the disadvantages of the optical detection method are its high technical effort and its disability to detect fault arcs within the single panels.

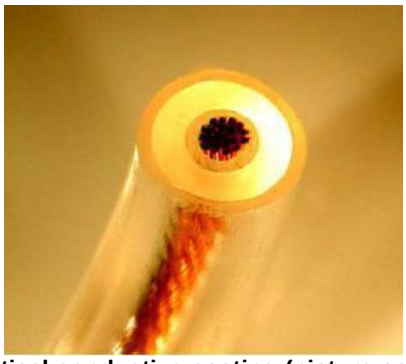

Figure 24: Power cable with optical conductive coating (picture source: Nordhausen University of Applied Sciences)

Some detection devices using optoelectronics are already commercially available. **Figure 25** depicts such a device from the company of DSL electronic GmbH.

Figure 25: Arc Detection Relay with optoelectronic evaluation unit (picture source: [10])

The so called SELCO D 1000 Arc Detection Relay is by manufacturer information to detect the arc within 1 ms. For the detection either photodiodes as punctual sensors for the monitoring of an area of 2 meter radius connected to the detection unit via 10 meters of shielded wire. Or a flexible optical fibre cable with a light sensitive length of 8 meters can be used to monitor a wider area like the section of an electrical cabinet [10]. **Figure 26** shows the photodiode sensor and the optical fibre cable.

Figure 26: Photodiode sensor and optical fibre cable for optoelectronic arc detection unit (picture source: [10])

5.3 FREQUENCY SPECTRUM BASED DETECTION METHODS

The most common method in arc detection is the measurement of the frequency spectrum of voltage and current. In photovoltaic and other DC systems there are basically two possibilities for the occurrence of a fault arc, either in series with the pv-generator (electric load in case of a supply network) or parallel to it (see section **4.1** and **4.2** for details). Both possibilities pose different hazards for the system, so a detection of both cases is inherently necessary. Generally, measuring the line current is fit to detect series fault arcs whereas the voltage needs to be supervised to detect fault arcs occurring parallel to the load/generator. As it was described in section 4, especially for series fault arcs need special emphasis for the protection, because the drop of voltage and the fault current level are not high enough to trip conventional fuses or safety devices. The changing property of the fault arc's plasma causes the so called pink noise (1/f noise).

To supervise voltage and current along a power cable either one-point or two-point measurement is applicable. Especially to capture the high frequency parts of current and voltage in case of a one-point measurement, capacitive or inductive sensors are used, for example the measurement of current is done by a Rogowski coil through the emitted electro-magnetic field of the cable. Because of the high inverter input capacity, the inductive coupling in the current path is more advantageous than a capacitive coupling of the voltage path. The resulting signals strongly vary in dependence of the applied inverter topology and EMC filters on the DC side [14]. **Figure 27** shows the schematic layout of a printed circuit board with a Rogowski coil on the upper left edge.

The analysis of the frequency spectrum exhibits an ambitious challenge for the signal processing, because the signal sequence of the noise is choked depending on the distance between the fault arc and the detection device. Further noise components that need to be distinguished from the fault arc noise is the noise spectrum caused by the inverter, the pulse frequency of the inverter and high frequency inputs from the pv-generator itself and the connecting cables [8]. Another critical intake is the portion of noise generated by switching operations in the grid which also lead to arcing, but in a controlled manner. Noise intakes from lightning strokes could also be critical for arc detection units in DC supply systems, because this intake can lead to a faulty activation of circuit breakers. All in all, the requirements for the detection algorithm are extraordinary high.

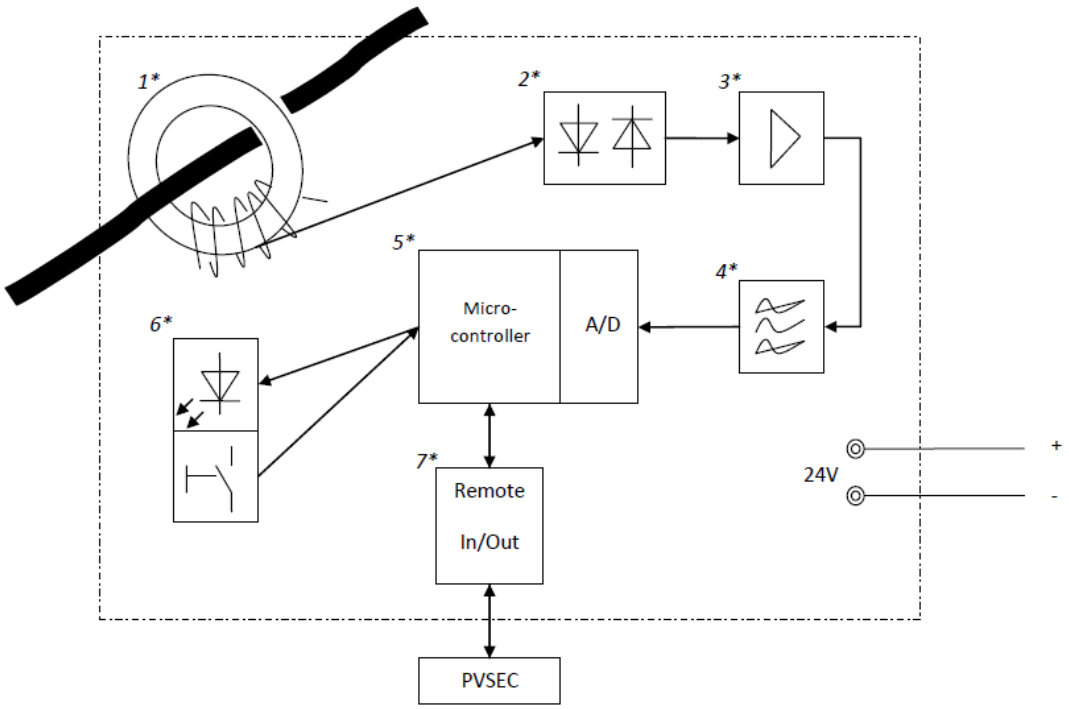

Figure 27: Layout of a printed circuit board to measure the frequency spectrum of voltage and current (picture source: [6])

Several algorithms for the pattern recognition to detect arc faults have been developed recently. Those algorithms are based on the fact that the frequency spectrum of arcs occurring because of switching operations in grid connected devises and gas-discharge lamps and other effects like electro-magnetic irradiation and crosstalk do have a different characteristic in the frequency domain than arc faults. **Figure 28** shows the frequency spectrum of the current in case of a series arc fault and normal operation for the PV-system test case in section 4. It is clearly visible that the spectrum in case of an occurring series fault arc differs significantly.

An example for an algorithm used to analyze the frequency spectrum is the wavelet transform. The wavelet transform of a signal is a degree of the similarity between the signal and a set of translated and scaled versions of a “mother wavelet”, which is a chosen fast delaying function. For further information on different algorithms for fault arc detection and its implementation see [11, 12, 13].

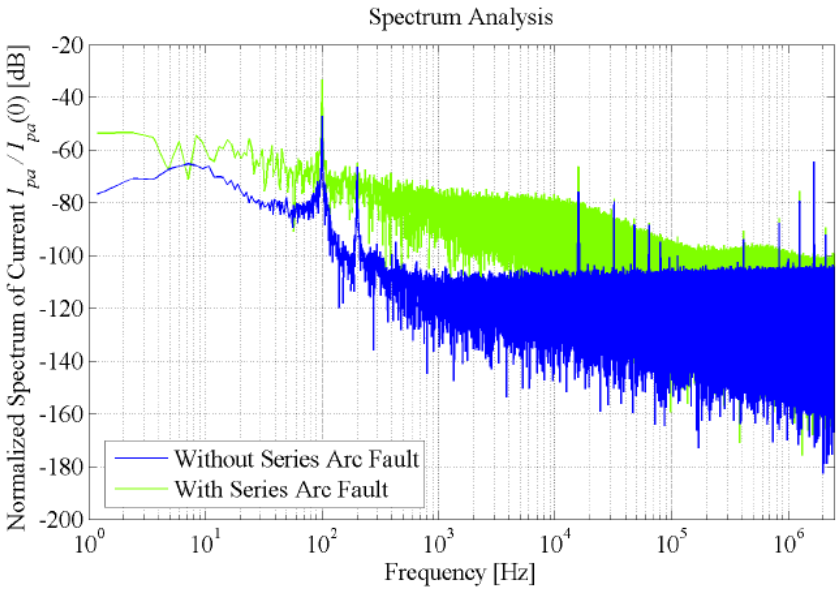

Figure 28: Comparison of current frequency spectrum in case of series arc fault and in normal operation (picture source: [8])

An additional problem is that the shape and magnitude of the detected current signal is strongly dependent on the distance between the arc fault location and the detection device. This distance defines how strong the signal is superposed by the noise of other grid components. **Figure 29** illustrates this circumstance.

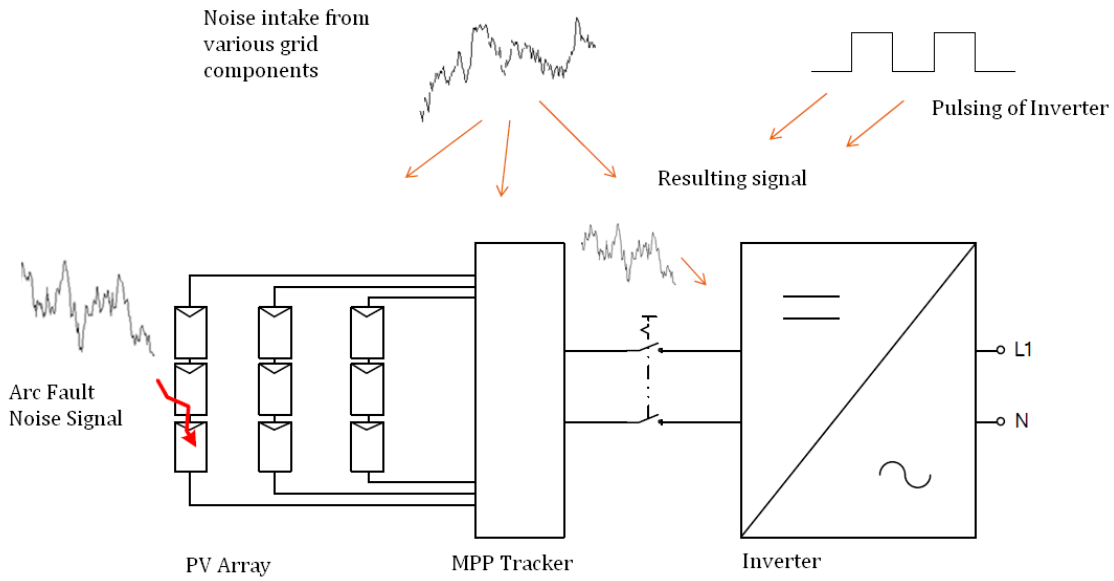

Figure 29: Distortion of arc fault noise signal by various grid components (picture source: [9])

Several industries besides the regenerative energy sector are confronted with the problem of detecting arc faults when operating DC systems with high voltages, e. g. the automotive and the aerospace industry where on-board systems are operated with high dc voltages to improve the overall efficiency. The following **Table 2** gives a brief overview on granted and pending patents in the field of fault arc detection.

Table 2: Selected patents on fault arc detection [9]

Number	Description
DE 101 55 796 B4	Current segmentation
DE 10 2004 051 734 A1	Optical arc detection
WO 2010/072717 A1	Analysis of ultra-sonic oscillations
WO 95/25374	Detection of characteristic radio waves
DE 10 2004 056 436 A1	Change of the circuit resistance
US005185687A	Comparison of the EM-field with chaos
US006683766B1	Detection of current irruption
DE 692 31 066 T 2	Detection of the voltage signal noise
EP 2 040 348 A2	Current monitoring and discrete Fourier transform (DFT)

5.4 TECHNICAL STANDARDS

In this context, it is necessary to take a brief look at technical standards. Due to the fact that the field of low voltage dc grids is comparably new the number of existing standards is straightforward. For example IEC 60364-7-712 and DIN VDE 0100-712 require a circuit breaker in every pv-system, but do not give further information where to install it. Therefore, the circuit breaker is often integrated in the inverter. This leads to the problem that in case of a fault some dc parts of the system would remain under high voltage. A better idea would be to locate several circuit breakers close to the panels which can be remotely tripped for example by fire fighters [4].

Referred to the detection units arc fault circuit interrupters (AFCI) there has just been an outline of investigation for a technical standard by the NEC (Article 690.11, UL 1699B). This investigation aims at the need of arc fault detectors for parallel and series arcs if the system voltage is exceeding 80 V_{DC}. The required tripping times of the AFCIs thereby are in the range of 0.8 s at 900 W arcing power and 2 s at 300 W arcing power. Looking at international standardization organizations, the IEC committee 23E, WG 2 is working on a standard for Arc Fault Detection Devices (AFDD).

6 ARC MANAGEMENT BY USING POWER ELECTRONICS

In a DC microgrid in which almost all loads are connected to the DC bus via a DC/DC converter. In consequence, the issue of arc management and clearance needs to be considered wisely. A problem like the one displayed in **Figure 30** where a series arc fault occurs in a feeding cable of a luminaire could be managed by power electronics for a safe shut-down of the system. After the detection of the fault with the help of methods described in the previous chapters either the affected load needs to be safely disrupted from the grid or the clearance of the arc fault needs to be done via a short-break of the whole system. In case of the first option, it is necessary to determine in which feeder the fault occurred. In the second case the power electronic circuitry of all connected devices needs to be able to handle such a short-break. The length of the short-break needs to be chosen long enough to enable a safe clearance of the fault arc and needs to be further discussed. It must be assured in this case, that the connected capacitances will not discharge into the arc fault during the short-break (see section **6.2**).

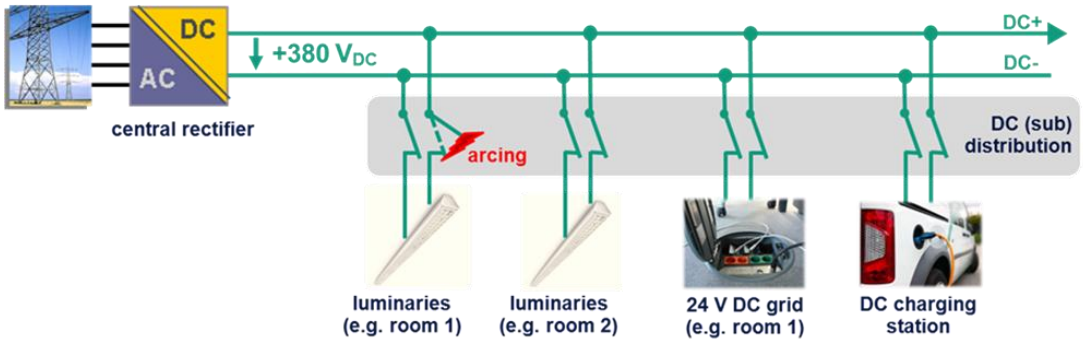

Figure 30: Arc fault situation in a DC supply system

To examine the behaviour of the system in an arc fault case, the office test bed at Fraunhofer IISB will be equipped with a measurement setup to create artificial arc faults in the system and evaluate both arc detection and various power electronic devices. **Figure 31** gives the mechanical setup of the arc fault generator. During the test period of the office building demonstrator the structure of the DC grid protection system needs to be designed to react correctly under the occurrence of any possible fault condition to proof the feasibility of low voltage DC grids in commercial and retail facilities.

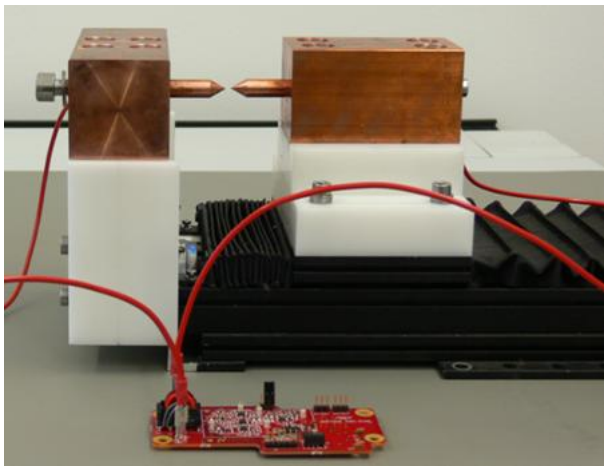

Figure 31: Arc fault generator

6.1 IMPACT ON DC/DC-CONVERTER TOPOLOGIES

Three common circuit topologies, that are adaptable for the use in low voltage DC grids, are displayed in **Figure 32**. The 4-switch topologies are well suited to connect overlapping voltage levels. For the connection of a DC source like pv-generators or battery storages to the high voltage DC bus, one would tend to select the half-bridge converter which is the easiest and most efficient of the three displayed topologies.

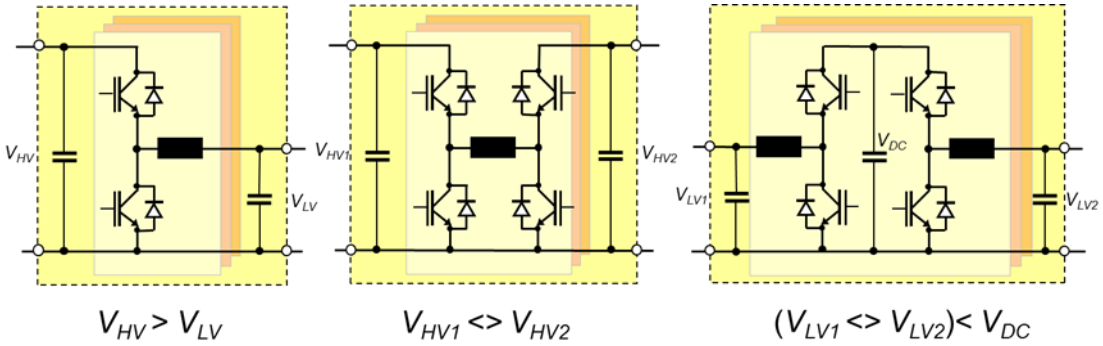

Figure 32: Half-bridge converter, full-bridge converter with inductive link and full-bridge converter with capacitive link

But there are several problems connected with the use of the half-bridge (buck/boost) converter depending on the voltage level of the dc source or energy storage in relation to the voltage level of the HV DC bus. This issue is inherently critical in case of a shut-break of the bus. For example, if the voltage of the DC source/energy storage is selected lower than the voltage level of the bus a boost-derived connection to the DC bus will be preferred. In this case, a short break of the system cannot be performed because of the included free-wheeling diode of the high-side switch. The problem is displayed in **Figure 33**.

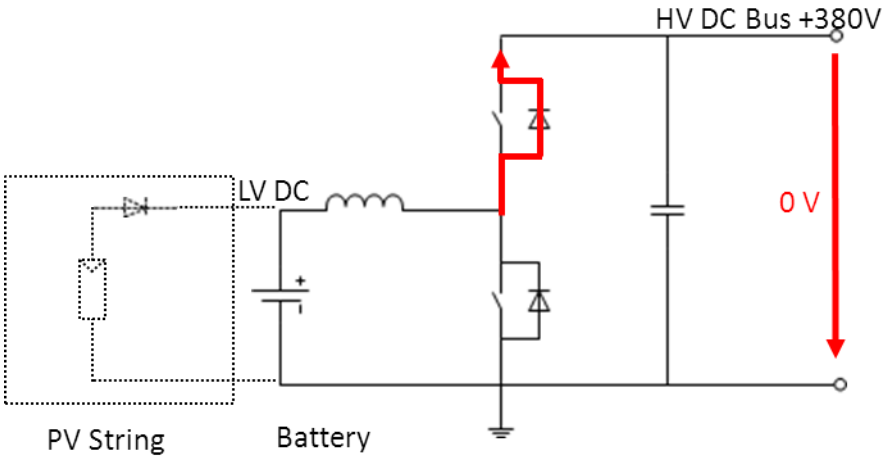

Figure 33: Connection of DC source/battery storage on low voltage side of half-bridge converter

The shut-down of the DC bus voltage will cause all capacities connected to the grid to discharge and to contribute to the resulting short-circuit current. In the depicted configuration, the resulting current flow out of the DC source/battery cannot be interrupted. This will result in an extraordinary high current flowing over diode of the high-side switch causing it to be damaged.
Another possibility would be to choose a higher voltage level for the DC source/battery and connect it to the high voltage side of the converter. This case is shown in **Figure 34**.

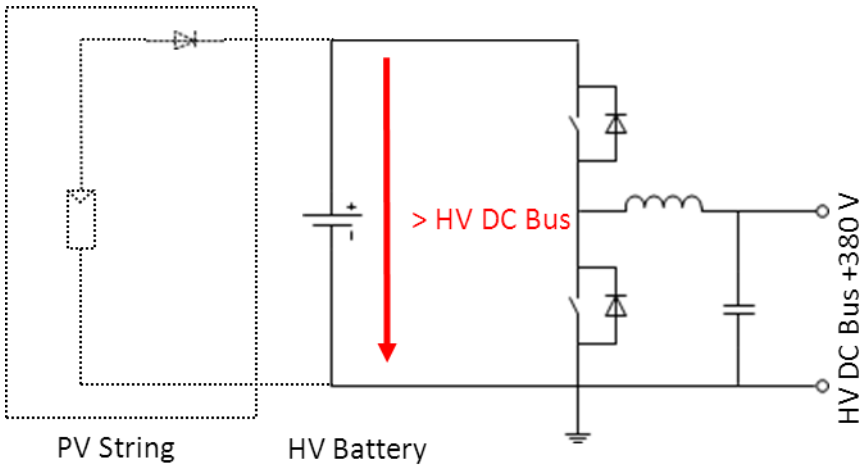

Figure 34: Connection of DC source/battery storage on high voltage side of half-bridge converter

This kind of connection enables a short-break of the DC bus voltage without damaging the converter, but due to the high voltage level of the DC source/battery storage (typically > 600 V_{DC}), this realisation requires semiconductor power switches inside the converter with a high breakdown voltage like the 1200 V micro pattern trench IGBTs that are developed by Infineon within the DCC+G project.

Additionally, a connection of components to the DC bus is always possible with converter topologies that provide galvanic insulation, like the resonant converter. These kinds of converters provide additional safety, but are more complex to realise and consequently more expensive and less efficient.

6.2 REQUIREMENTS FOR INPUT AND OUTPUT CIRCUITRY OF THE DC GRID APPLIANCES

The design of input and output circuits needs special attention. The goal should be to design the input circuitry in a way that short-breaks with durations of e.g. 10 ms can be handled by the components without affecting their operability (if this is needed for the application). In the DCC+G deliverable D1.1.3 [16] it is demanded that the whole system needs to have the capability to clear any occurring fault condition within 20 ms. By using central arc detection and management this means that during this time all capacitances with a direct connection to the DC bus must be discharged or disconnected. To reach this feature, the overall bus capacitance should be as low as possible.

For the input circuitry of the loads, **Figure 35** shows that a diode for inverse polarity protection and a fuse against over currents are included into the feeding cable. With this make-up the overall bus capacitance can be reduced, because in a fault case, the diode prevents the reverse flow of energy out of the load into the DC Bus. The hold-up time for the loads can therefore be increased, but with the disadvantage of a lower overall efficiency due to the power losses in the diode. In the DCC+G deliverable D1.1.3 [16] the value of the input capacity for each application is proposed to be 1 µF/W.

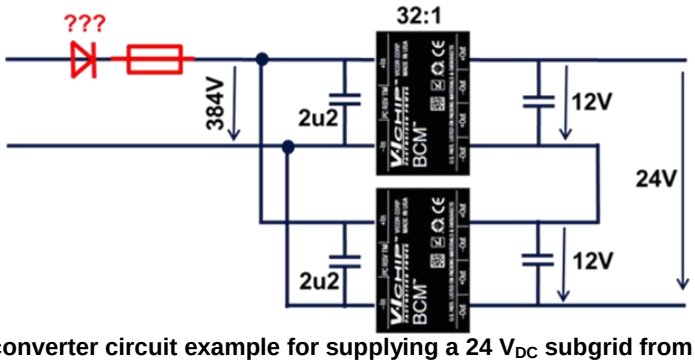

Figure 35: DC/DC converter circuit example for supplying a 24 V_{DC} subgrid from the HV DC bus

In contrary, a compromise has to be found for the output circuitry of the central rectifier and all power generators of the system. On the one hand, the output capacitance of these components must be high enough to provide sufficient short circuit currents to trip fuses and to enable the system to overcome short-breaks in case the supplying AC mains fail. On the other hand, in case of a series arc fault, the discharging of the capacitances into the fault arcs needs to be prevented.

To meet these requirements an arc management circuit was designed and evaluated in a simple LT spice simulation. The schematic is displayed in **Figure 36**.

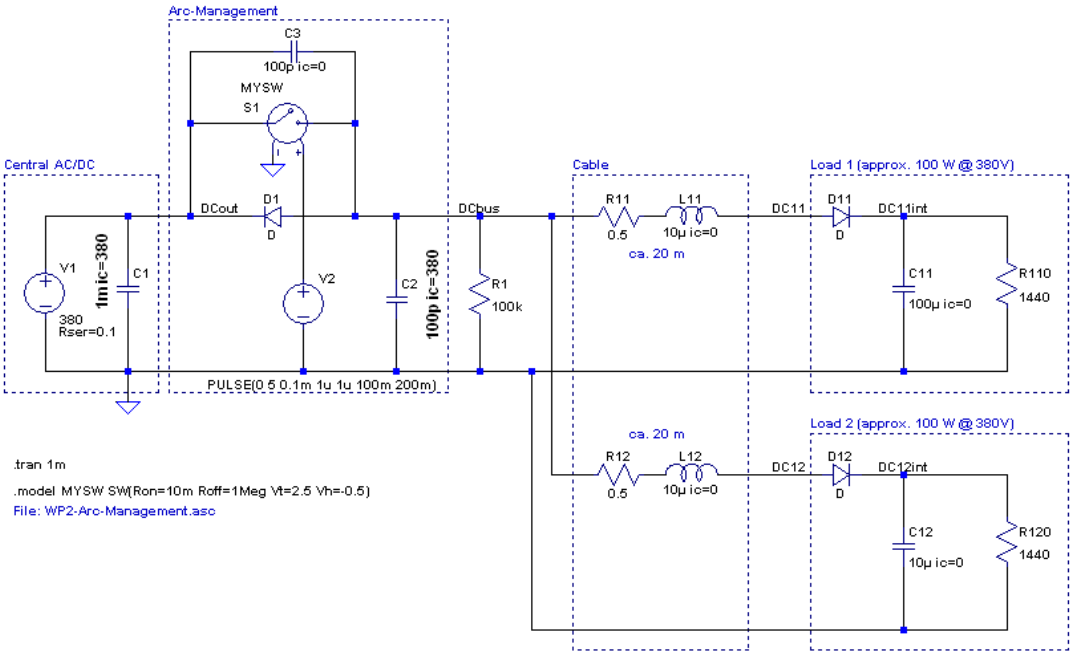

Figure 36: Schematic of simplified simulation model for switch-on case

The two loads were modelled to have a constant resistive behaviour. The central rectifier was modelled as a constant voltage source with an output capacitance of 1 mF. The inductance and resistance of the 3 x 1, 5 mm^2 NYM (*R'*= 23 mΩ/m, *L'*= 0.41 µH/m) cables that are used to connect the loads were also taken into account.

The arc management circuitry consists of the diode D1 connected in opposite direction of the nominal current direction. The capacitance of the diode was considered with capacitor C3. D1 is bypassed by the switch S1 under normal operation. The switch only opens in case of a fault or short-break. C2 was included to simulate some capacitance on the HV DC bus. Both, C2 and C3, were assumed to have a capacitance of 100 pF. Resistor R1 with 100 kΩ accounts for connected measurement equipment on the DC Bus.

For the first simulation two equal loads each with a consumption of 100 W were assumed. To make an appropriate statement about inrush currents for different values of the input capacities, one load was considered to have the demanded capacitance of 100 µF, the other one was considered to have a reduced capacitance value of 10 µF. The simulation result can be found in **Figure 37**.

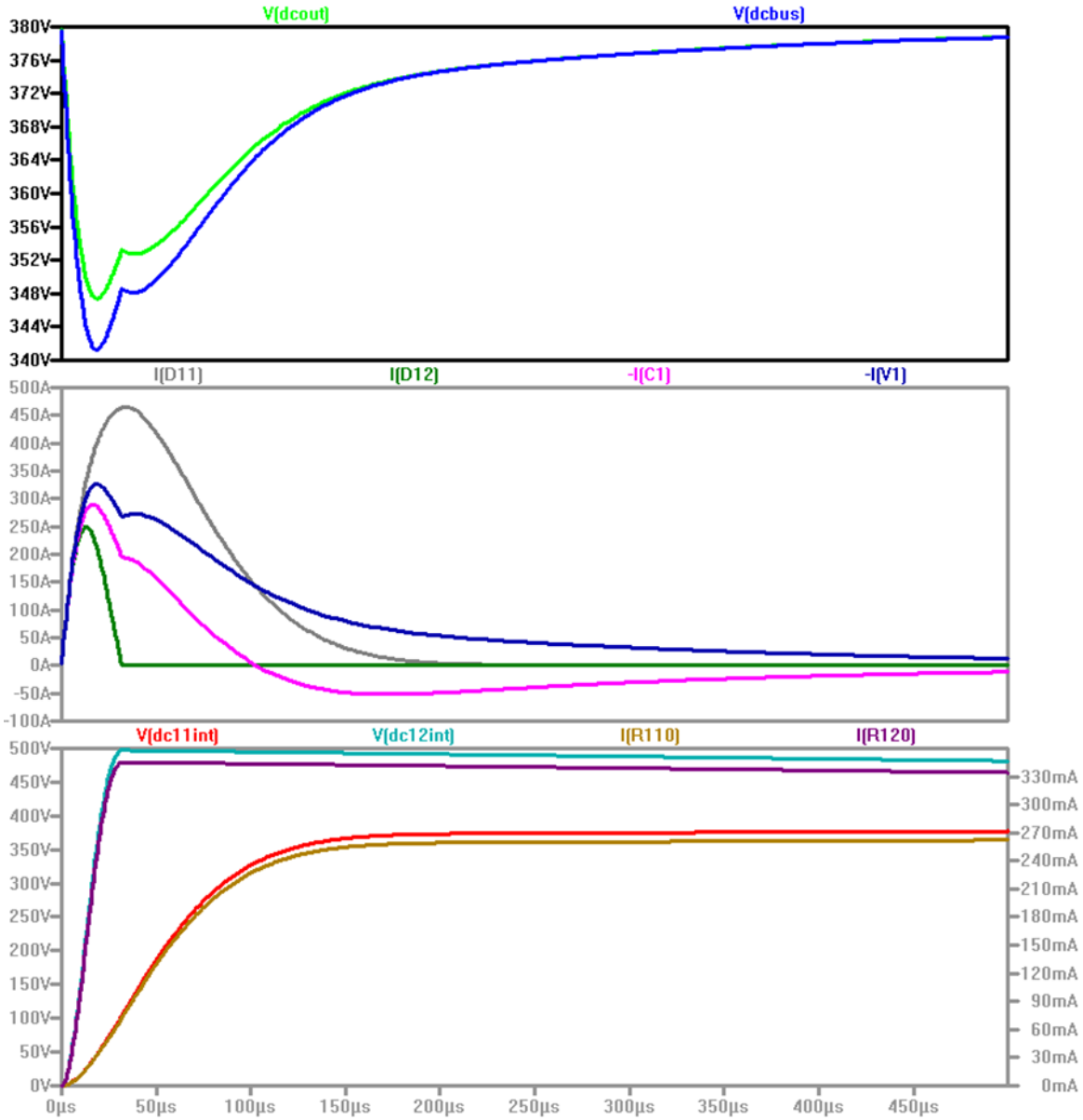

Figure 37: Simulation of switch-on behavior for two loads (100 W @ 380 V) with 100uF respectively 10 uF input capacitance

The simulation shows the switch-on of both loads at the same time by switching on S1. This causes the DC bus voltage to drop to a value of about 340 V (the internal resistance of the voltage source V1 is assumed to 100 mΩ). The inrush current of load 1 with 100 µF input capacitance reaches a peak value of slightly over 450 A. For load 2 with a reduced input capacity the input current peak is about 250 A. These high inrush current values probably are too high to be handled by solid state relays that use only one single power electronic switch rated to the nominal load current. So, more switches have to be connected in parallel.

Other possibilities to reduce the inrush current values are the use of some sort of pre-charge circuit that charges the input capacitances of the loads before they are connected to the DC bus or to use some inrush current limiting circuits.

6.3 OVERVOLTAGES DURING A SHORT-BREAK

For the load 2 with the reduced input capacitance the resulting overvoltage poses an additional issue. Even if a lower input capacitance reduces the inrush currents, the switch-on overvoltage increases significantly. This is also extraordinary critical for all kinds of semi-conductor switches and emphasises the need for pre-charging of the load capacitances.

For the next simulation case, load one was increased to a value of 1 kW. The input capacitance for load 1 is again 100 µF, for load 2 (still 100 W) it is 10 µF. The simulation setup can be found in **Figure 38**.

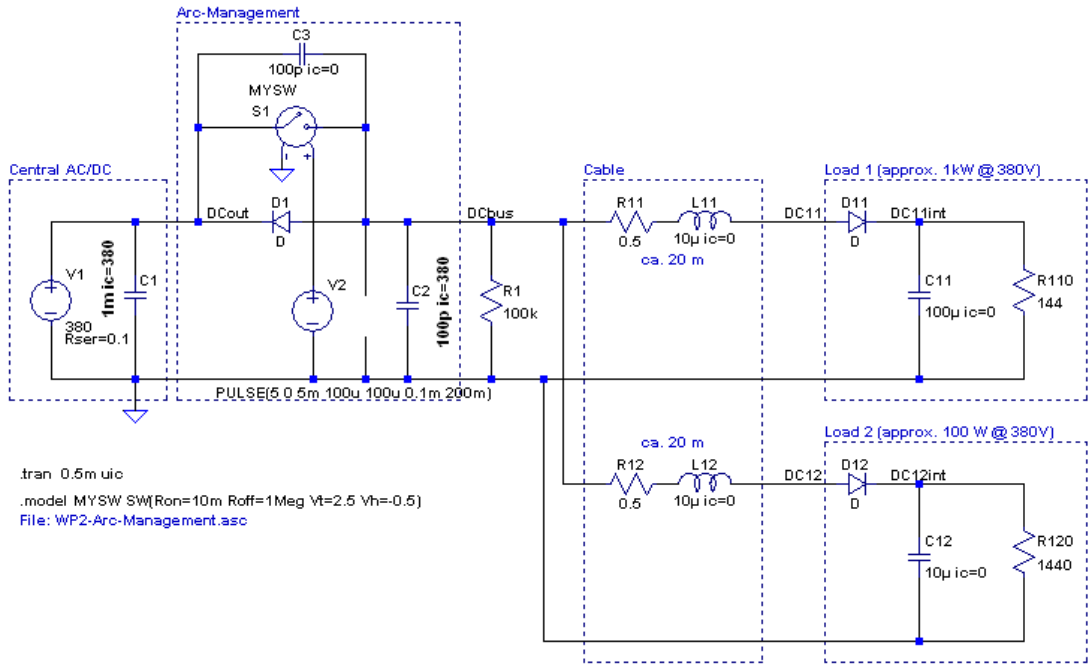

Figure 38: Schematic of simplified simulation model for switch-off case

In this simulation the fast switch-off behavior of the system is considered, e. g. in case of a detected series arc fault. The results can be seen in **Figure 39**. In this case, the switch-off time of S1 was selected short. It can be seen from the curves in the topmost diagram that this fast switch off leads to over voltages on the central DC bus due to the resulting high dI/dt in inductance L1 and L2.. Also this could be problematic for several connected components.

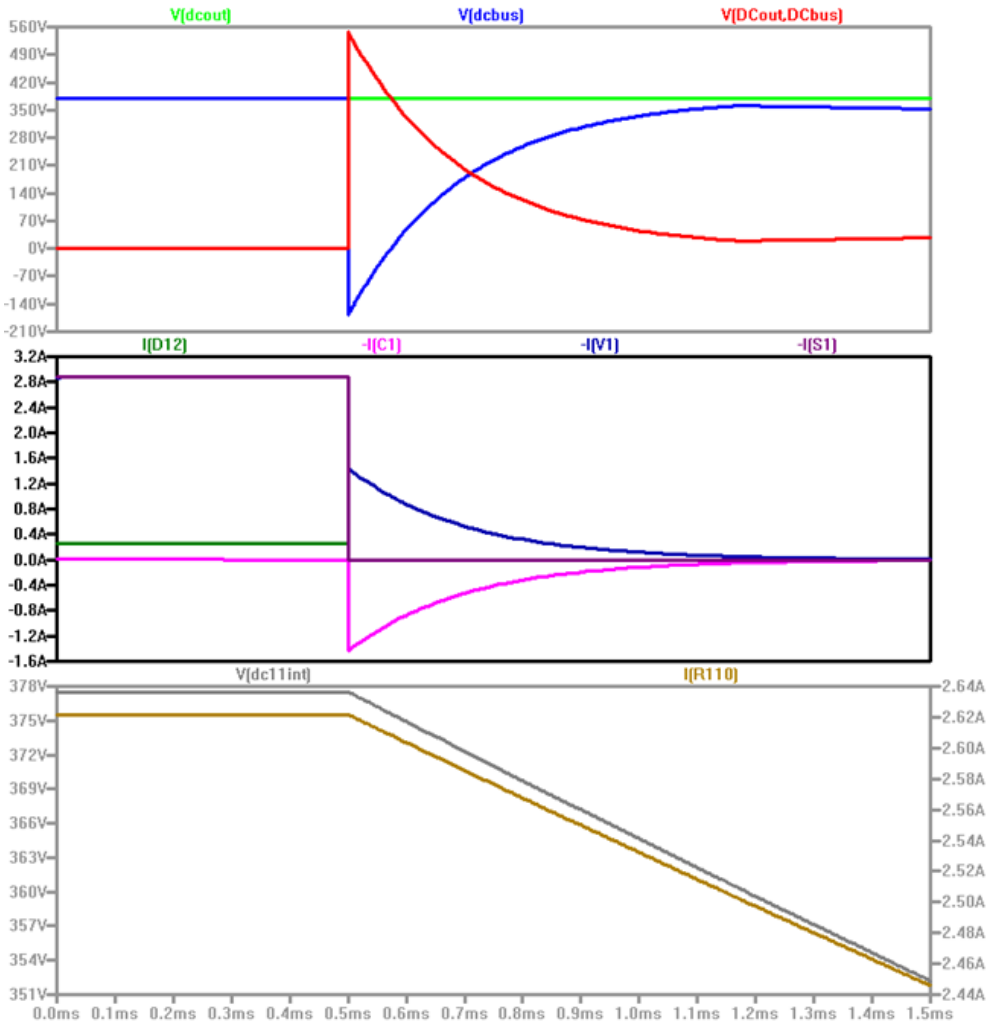

Figure 39: Simulation results for a short switch-off time for S1 in the case of a system failure (e.g. detected arc)

To reduce the over voltage the switch-off time can be increased. The simulation results are displayed in **Figure 40**. The slow switch-off time will cause high power losses in S1 but this is not a problem, because this happens only in the case of a fault.

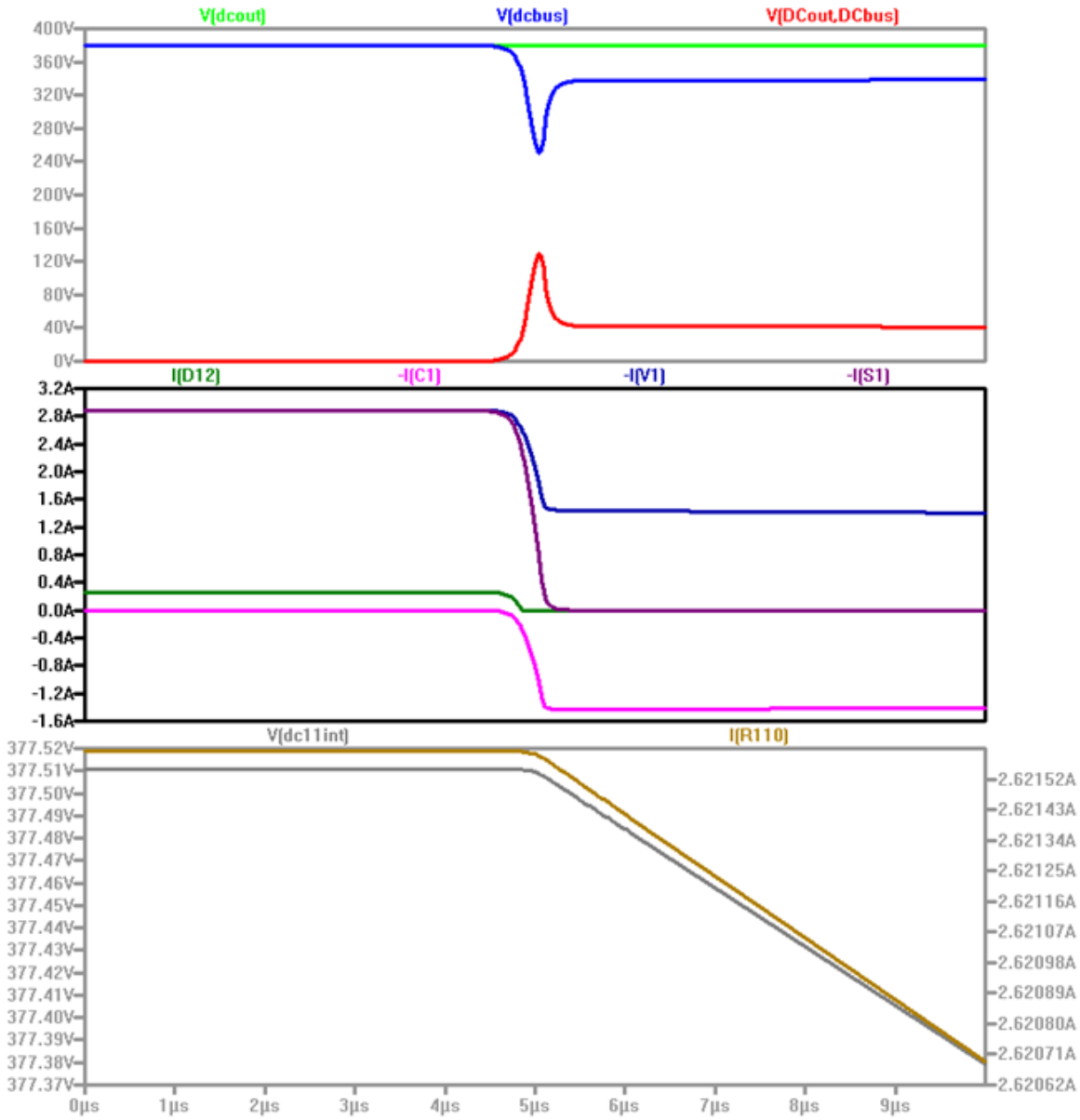

Figure 40: Simulation results for a long switch-off time for S1 in the case of a system failure (e.g. detected arc)

Of course, after the fault (e.g. arc) is cleared, the problem of high inrush currents arises again. The needed time to clear the fault is therefore the critical parameter, because it defines the amount of load that is discharged from the load input capacitor and that needs to be recharged when the system is switched-on again.

As can be seen from **Figure 41** the inrush currents after a short-break of 1 ms already reach significant values even for small capacitances of 10 µF. Like in the case for the start-up of the system, for longer lasting short-breaks of the system some sort of pre-charge circuit is required.

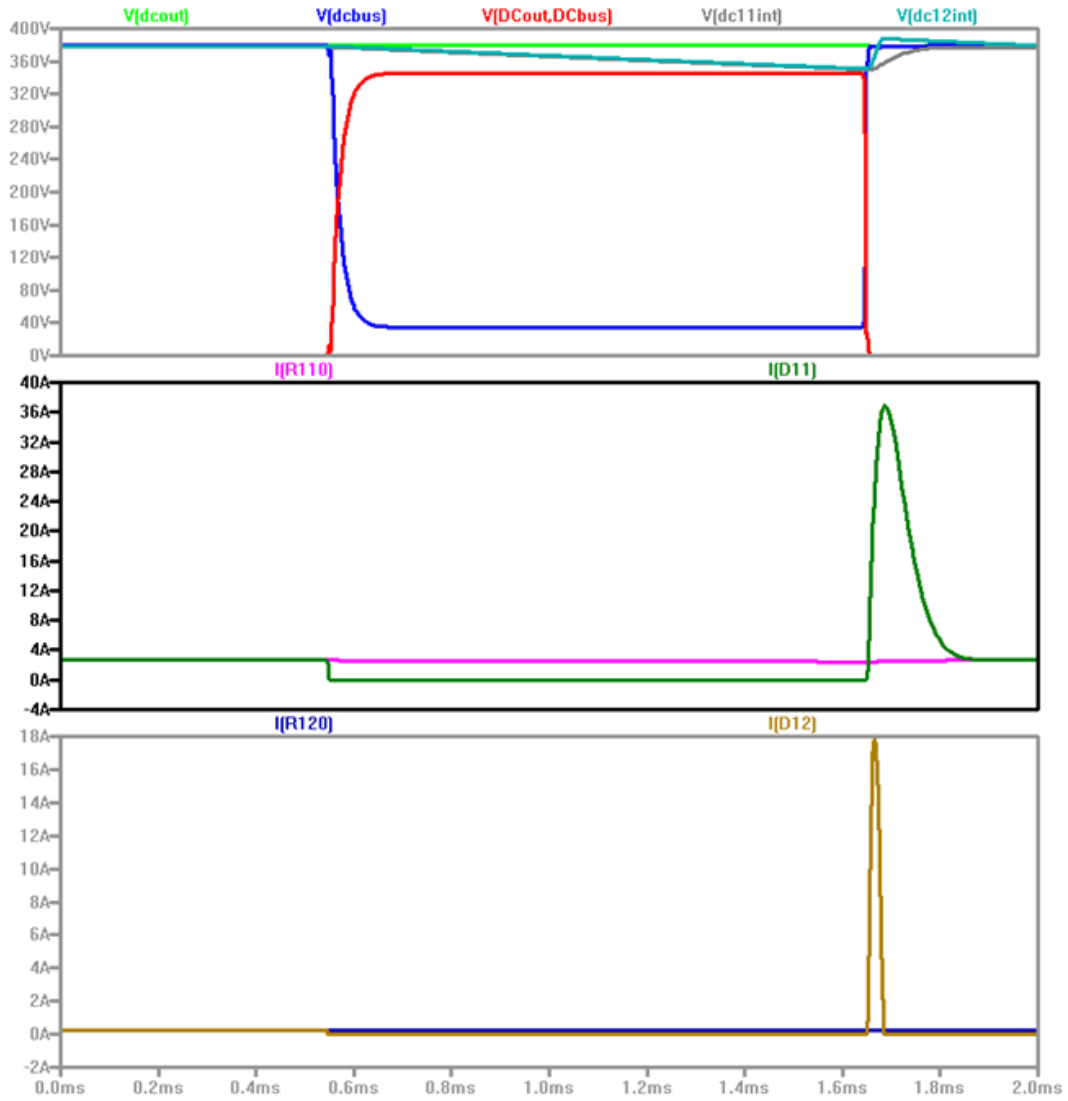

Figure 41: Simulation results for a short-break time of 1 ms

Figure 42 gives the results for short-break of 0.2 ms. As it was already presumed, the inrush currents are reduced to a moderate level for both loads. But it needs to be proven, if the duration of the short-break is sufficient to clear all kinds of arc faults.

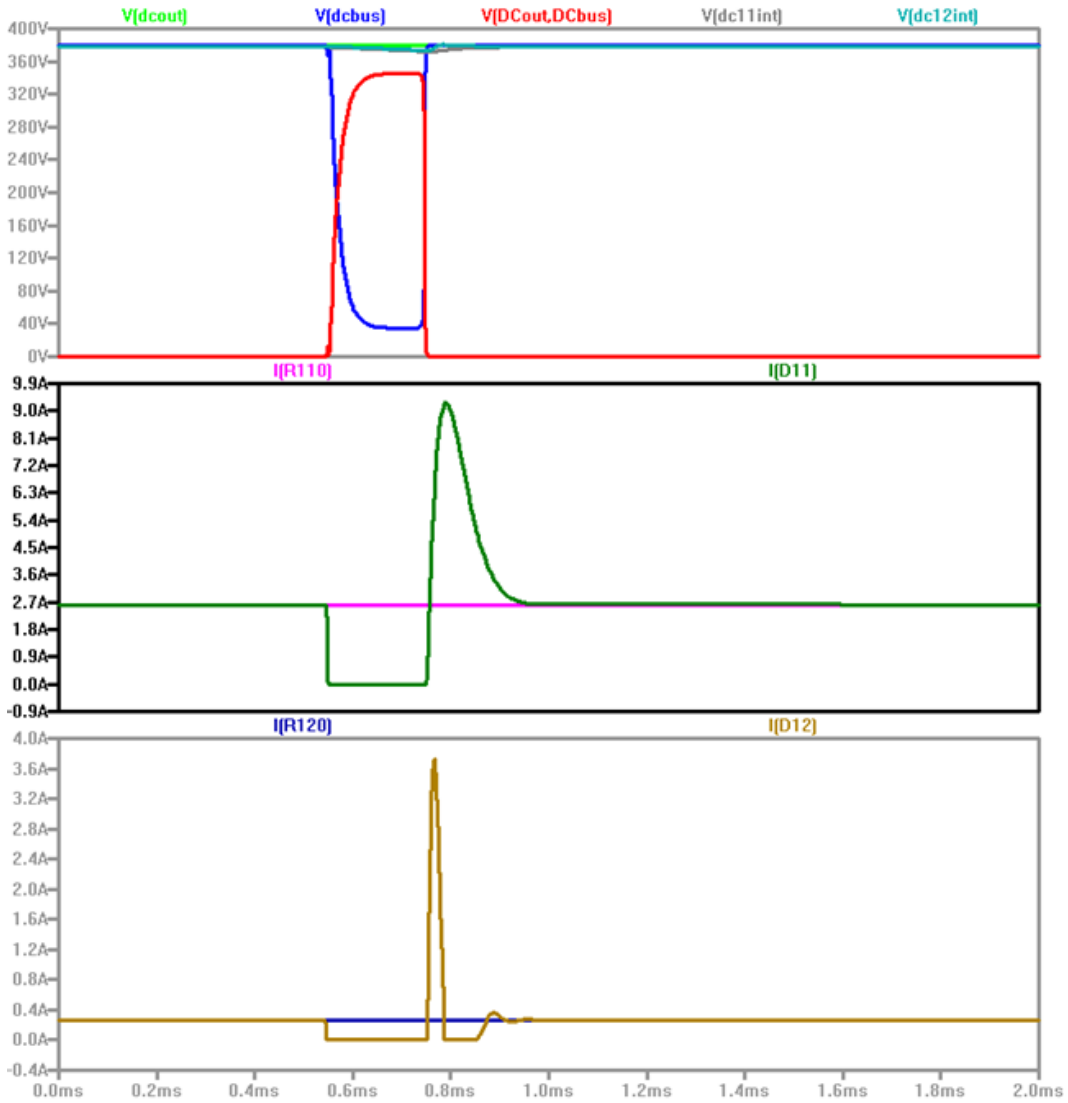

Figure 42: Simulation results for a short-break time of 0.2 ms

Figure 41 shows that only with a very short break time and the assumption of relative low loads (e.g. 100 W – see current through D12) and very low input capacitors the problem of inrush currents after switching-on the DC bus again could be managed without special inrush limiting circuits.

6.4 LOCATION OF ARC DETECTION

By using a central arc detection unit on the HV DC bus nearly the whole DC grid can be supervised, because it is possible to detect arcs in subnets that are connected via mechanical or solid state DC relays. Unfortunately this is much more difficult in subnets that are connected via DC/DC converters due to their switching behavior and it is not possible in subnets that are connected via galvanic isolated DC/DC converters.

Figure 43 shows the situation with a central arc detection unit on the HV DC bus for the office test bed.

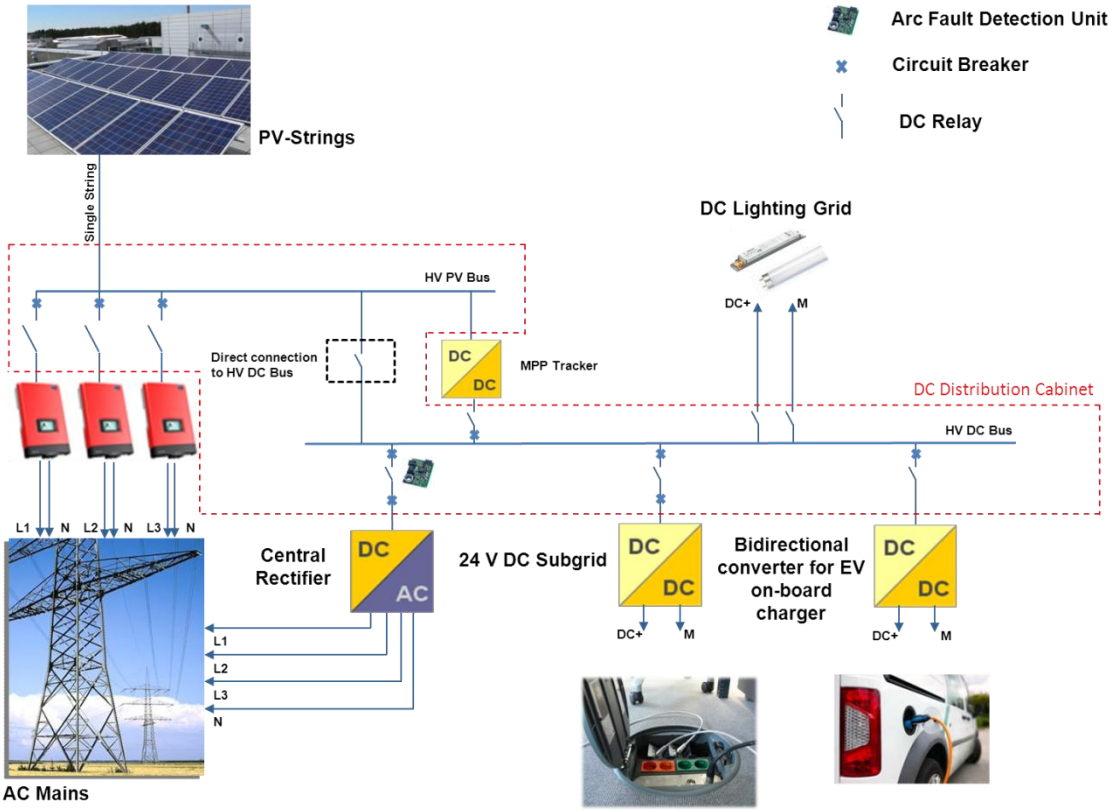

Figure 43: Office test bed microgrid with central arc detection unit on the HV DC bus

The major disadvantage of only one central fault arc detection unit is the fact that in case of a fault the entire system needs to be shut-down. This is necessary, because the location of the fault arc cannot be determined accurately enough to decide whether the central DC bus is affected by the fault or just one feeder of the microgrid.

A better solution would be to install fault arc detection units in every feeder. Of course, this will make the protective system a more complex for a signal processing and control unit is needed to interpret the signals from the detection units. But, this kind of protective system significantly increases the reliability of the system, because unless the central DC bus is affected only the feeders in which the fault was detected can be short circuited by means of power electronics without having an impact on the other feeders of the grid. **Figure 44** gives an idea how the office test bed microgrid can look with distributed fault arc detection units.

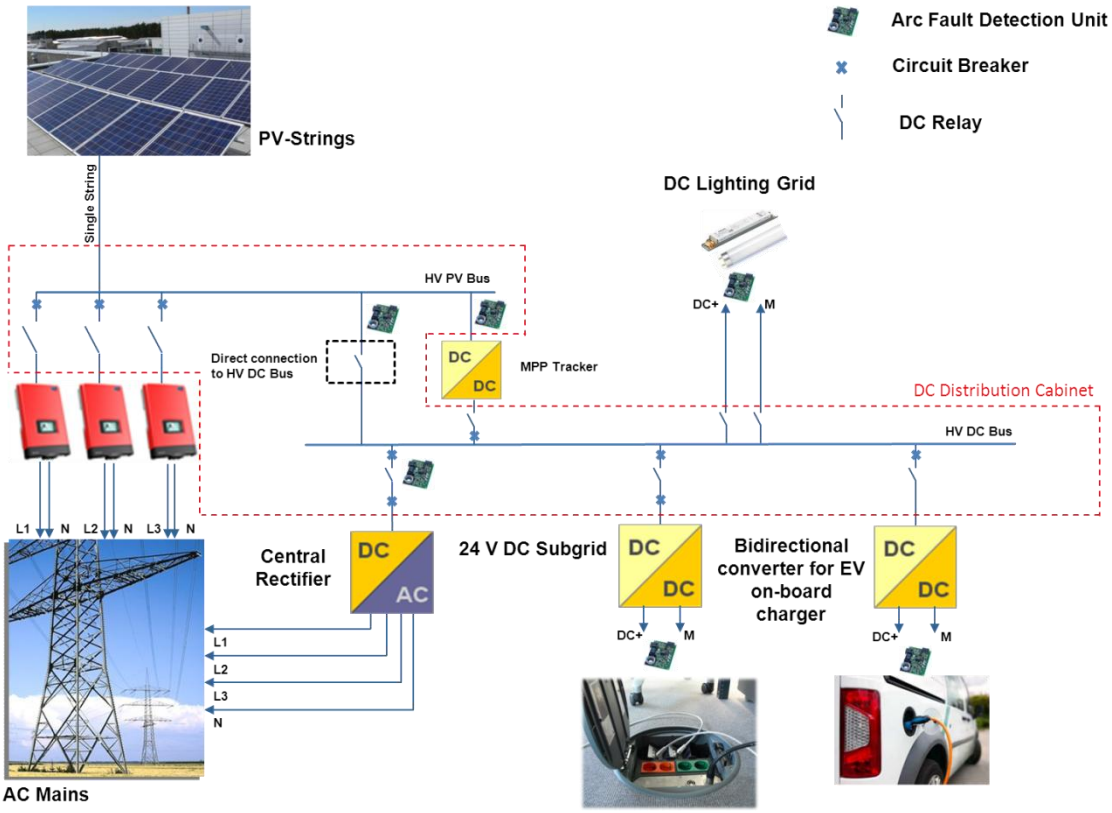

Figure 44: Office test bed microgid with distributed fault arc detection units

This proposed protection system allows “crowbarring” the fault. The protection of the DC circuit is provided by the normally installed short circuit protection devices.

7 SUMMARY

In this report the hazard potential of fault arcs for DC supply systems was analysed and methods to detect and clear the faults were presented. It was outpointed, that under certain circumstances an arc fault cannot be detected just by measuring the voltage and current (e.g. series fault arc in pv-systems) in the single branches of the microgrid. Therefore, more advanced and accurate detection methods which take the specific disturbing quantities of the grid into account need to be applied for a reliable detection of a fault.

Also, different kinds of switches for DC currents were described. In opposite to AC systems, switching actions in DC grids are much more complicated, because the switching arc is not cleared automatically by the zero crossing of the supply voltage in every half cycle. Therefore, sophisticated switch topologies need to be applied. It is strongly dependant on the expectable current and voltage strengths which topology fits best for a certain application. The presented hybrid switch from section 3.3 combines the advantages of both techniques and ensures a long life cycle.

By using simplified circuit simulations the basic behaviour of a DC grid which is switched on and off via power electronic devices could be investigated. It was shown that very fast switch-off should be avoided due to possible high over voltages especially at higher power levels. Moreover it was shown that possible inrush currents have to be considered. This is important especially in the case if a central arc management should be realized with a certain hold-up time for some applications.

The report focused exclusively on DC supply systems which do have the central rectifier and a pv-generator as sole energy sources. The considered loads were assumed to be electric only. The drawn conclusions of this report need to be revised, if also mechanical loads like fans or energy sources with rotating masses like Micro-CHP units are considered. The energy stored in the inertia or the inductances of these components also have to be dissipated in a safe manner. This problem needs to be addressed during the test phase of the demonstrators realized within DCC+G. The results need to be complemented then to this report.

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